Design Example Report

Title	***27 W USB PD 3.0 with PPS Power Supply Using InnoSwitch™ 3-CP INN3266C-H210 and Cypress CCG3PA CYPD3175***
Specification	85 VAC – 265 VAC Input; 5 V / 3 A; 9 V / 3 A; 3 V – 11 V PPS
Application	Mobile Phone Charger
Author	Applications Engineering Department
Document Number	DER-603
Date	August 9, 2018
Revision	1.3

Summary and Features

- USB PD 3.0 with PPS support via single secondary-side IC (CCG3PA CYPD3175)
- InnoSwitch3-CP is the industry's first AC/DC IC with isolated, safety rated integrated feedback
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
- Built-in synchronous rectification for high efficiency
- Meets DOE6 and CoC V5 2016 efficiency requirement (>1 % efficiency margin)
- Micro stepping of voltages and CC thresholds in compliance with PPS protocol
- Output overvoltage and overcurrent protection
- <30 mW no-load input power
- Integrated thermal protection

PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 27 W USB PD power supply which can be configured for 5 V / 3.0 A, 9 V / 3 A or 3-11V with adjustable voltage and current to comply with USB PD 3.0 and PPS protocol. This power supply uses the InnoSwitch3-CP integrated power supply controller from Power Integrations and Cypress CCG3PA (CYPD3175) USB PD controller. This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch3-CP controller providing exceptional performance.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data

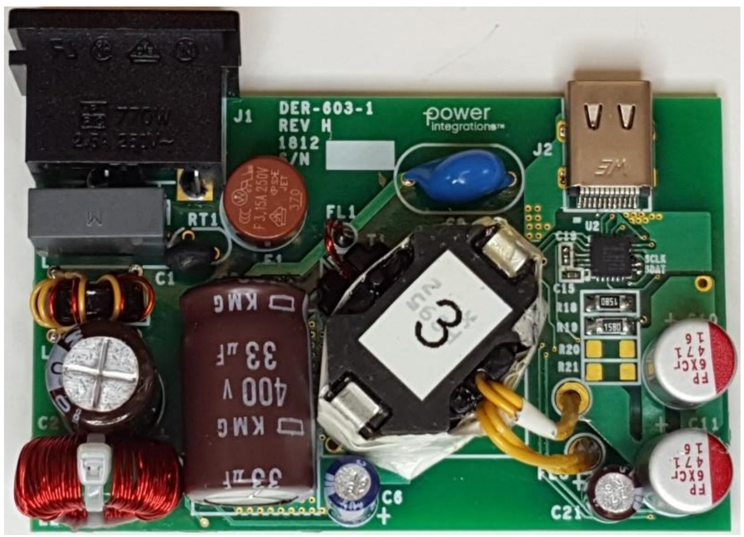

Figure 1 – Populated Circuit Board Photograph, Top.

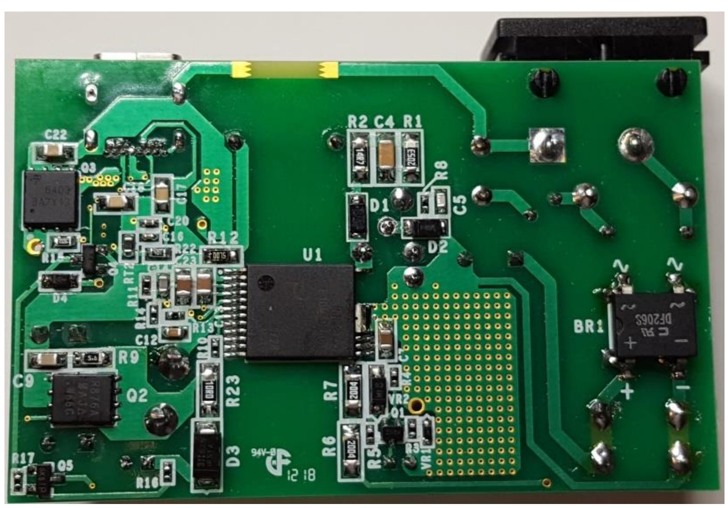

Figure 2 – Populated Circuit Board Photograph, Bottom.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (85 VAC)			25.1	27	mW	Measured at 85 VAC.
5 V Output						
Output Voltage	V_{OUT1}		5		V	±3%
Output Ripple Voltage	$V_{RIPPLE1}$			150	mV	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Output Current	I_{OUT1}	3.0		3.1	A	20 MHz Bandwidth.
Efficiency	η	81.8			%	
9 V Output						
Output Voltage	V_{OUT1}		9		V	±5%
Output Ripple Voltage	$V_{RIPPLE1}$			200	mV	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Output Current	I_{OUT1}	3.0		3.1	A	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Efficiency	η	87.3			%	
PPS Voltage Range	V_{OUT1}					
Minimum Programmable Voltage			3.0		V	Complies with USB PD3.0 PPS Specification.
Maximum Programmable Voltage			11.0		V	
Maximum Output Ripple (PPS Mode)	$V_{RIPPLE1}$			150	mV	For Voltage <6 V.
				200	mV	For Voltage >6 V.
Continuous Output Power	P_{OUT}	27			W	
Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		45	ºC	Free Convection, Sea Level.

3 Schematic

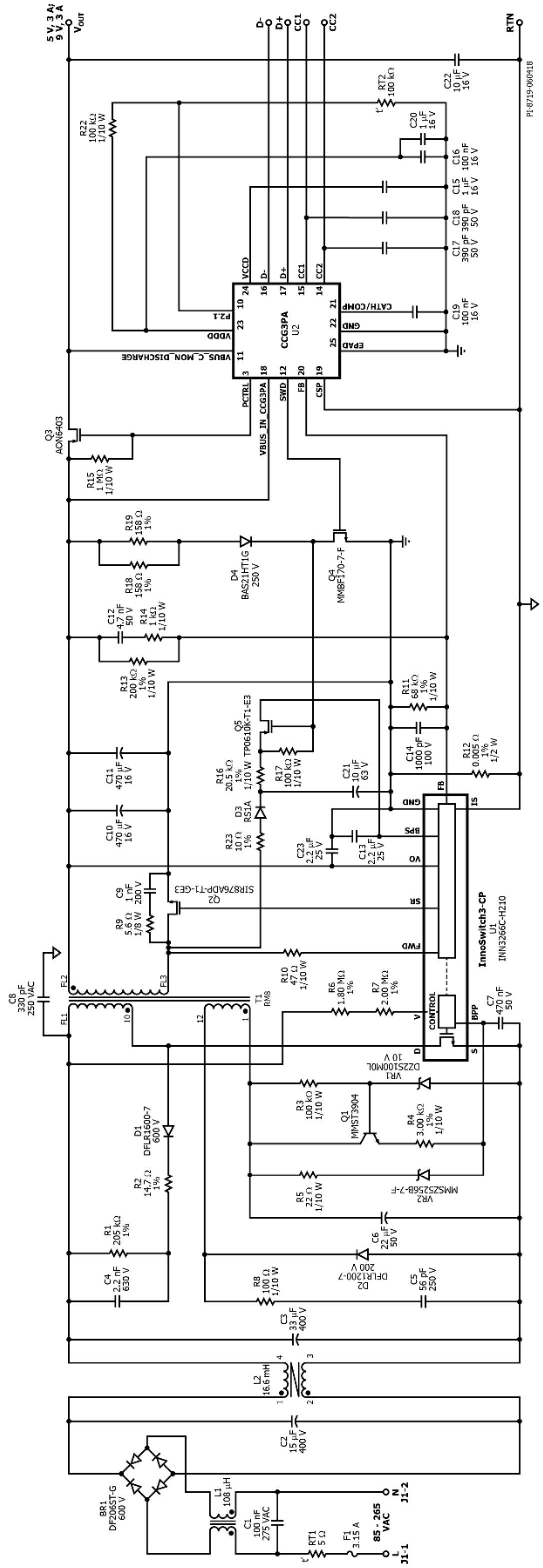

Figure 3 – Schematic.

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4 Circuit Description

4.1 Input EMI Filtering

Fuse F1 isolates the circuit and provides protection from component failure, and the common mode choke L1 with capacitor C8 provides attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter consisting of C2, L2, and C3. The inductor L2 and capacitors C2, C3 form a pi-filter. This filter provides differential and common mode noise filtering. Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply. X-capacitor C1 provides differential mode noise filtering.

4.2 InnoSwitch3-CP IC Primary

One end of the transformer primary is connected to the rectified DC bus; the other is connected to the drain terminal of the MOSFET inside the InnoSwitch3-CP IC (U1). Resistors R6 and R7 provide line undervoltage and overvoltage sensing for U1.

A low cost RCD clamp formed by diode D1, resistors R1 and R2, and capacitor C4 limits the peak Drain voltage of U1 at the instant of turn off of the MOSFET inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor (C7) when AC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C6. Resistor R4 limits the current being supplied to the BPP pin of the InnoSwitch3-CP IC (U1). A linear regulator comprising resistor R3, BJT Q1 and Zener diode VR1 limits the current through R4 for higher output voltages. The RC network comprising of resistor R8 and capacitor C5 offer damping to the high frequency ringing in the voltage across diode D2 which reduces radiated EMI.

Zener diode VR2 with series resistance R5 offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR2 which then causes a current to flow into the BPP pin of InnoSwitch3-CP IC U1. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch3-CP controller will latch off and prevent any further increase in output voltage.

4.3 InnoSwitch3-CP IC Secondary

The secondary-side of the InnoSwitch3-CP IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by MOSFET Q2 and filtered by capacitors C10 and C11. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RC snubber, R9 and C9.

The gate of Q2 is turned on by secondary side controller inside IC U1, based on the winding voltage sensed via resistor R10 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the MOSFET is turned off just prior to the secondary side commanding a new switching cycle from the primary. In discontinuous mode of operation, the power MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold of approximately 0 mV. Secondary-side control of the primary-side power MOSFET avoids any possibility of cross conduction of the two MOSFETs and provides extremely reliable synchronous rectification.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C13 connected to the BPS pin of InnoSwitch3-CP IC U1 provides decoupling for the internal circuitry.

During CC operation, when the output voltage falls, the device will power itself from the secondary winding directly. During the on-time of the primary-side power MOSFET, the forward voltage that appears across the secondary winding is used to charge the decoupling capacitor C13 via resistor R10 and an internal regulator. This allows output current regulation to be maintained down to ~3.0 V. Below this level the unit enters auto-restart until the output load is reduced.

Capacitor C23 between VOUT pin and GND pin provides protection for ESD for the VOUT pin.

4.4 **USB Type-C and PD Interface**

In this design, CCG3PA CYPD3175-24LQXQ (U3) is the USB Type-C and PD controller. Output of the InnoSwitch3-CP powers the CCG3PA device. The IS and FB pin of the InnoSwitch3-CP IC are directly connected to the CCG3PA IC. P-MOSFET Q3 makes the USB Type-C receptacle cold socket when no device is attached to the charger as per the USB Type-C specification. The gate of the P-MOSFET Q3 is directly driven by the CCG3PA IC. The discharge of the VBUS output after Q3 is also internally done by the CCG3PA IC.

USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which Type-C plug is connected.

Output current is sensed by monitoring the voltage drop across resistor R12 between the IS and GND pins with InnoSwitch3-CP maximum CC voltage threshold of approximately 35 mV. This threshold sets the maximum CC threshold for the power supply. The CCG3PA IC can adjust the CC threshold to any value between this maximum threshold and 1 A depending on the PDO request it receives from the sink side.

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Below the CC threshold, the device operates in constant voltage mode. Output voltage is regulated so as to achieve a voltage of 1.265 V on the FB pin. Resistor R14 and capacitor C12 form a phase lead network that ensure stable operation and minimize output voltage overshoot and undershoot during transient load conditions. Capacitor C14 provides noise filtering of the signal at the FB pin. Resistors R13 and R11 form the voltage divider network for the FB pin. The CCG3PA IC can adjust the FB pin voltage by sinking or sourcing current to it depending on the PDO voltage request it receives from the sink. The InnoSwitch3-CP IC will then increase/decrease the output voltage in response so as to regulate the FB pin voltage at 1.265 V.

The network consisting of N-FET Q4, D4 and resistors R18 and R19 present an active pre-load circuit for operations below output voltage of 4.7 V in order to sustain enough switching activity required for light load or no load operations for charging the BPS capacitor through the FWD pin. In order to reduce heat dissipation in the pre-load circuit, an additional circuit as described below is used to inject current in to the BPS capacitor to keep it charged at approximately 4.4 V.

The network consisting of R23, D3 and C21 act as a peak charge detector and feeds current to the BPS pin through resistor R16 once the P-FET Q5 is turned ON. The gate of the N-FET Q4 is controlled by the Cypress CCG3PA IC U2 and once Q4 turns ON, it pulls down the gate of the P-FET Q5 turning it ON. This is needed to keep the BPS capacitor voltage above its reset threshold voltage at light or no load operations for output voltages of 4.7 V – 3 V. This circuit is disconnected by turning off the FET Q5 for output voltage above 4.7 V, which helps to ensure extremely low no load power consumption and high efficiency.

The CCG3PA IC also provides output overvoltage and under voltage protection. It also provides output over current protection for fixed PDOs.

5 PCB Layout

PCB copper thickness is 2.0 oz.

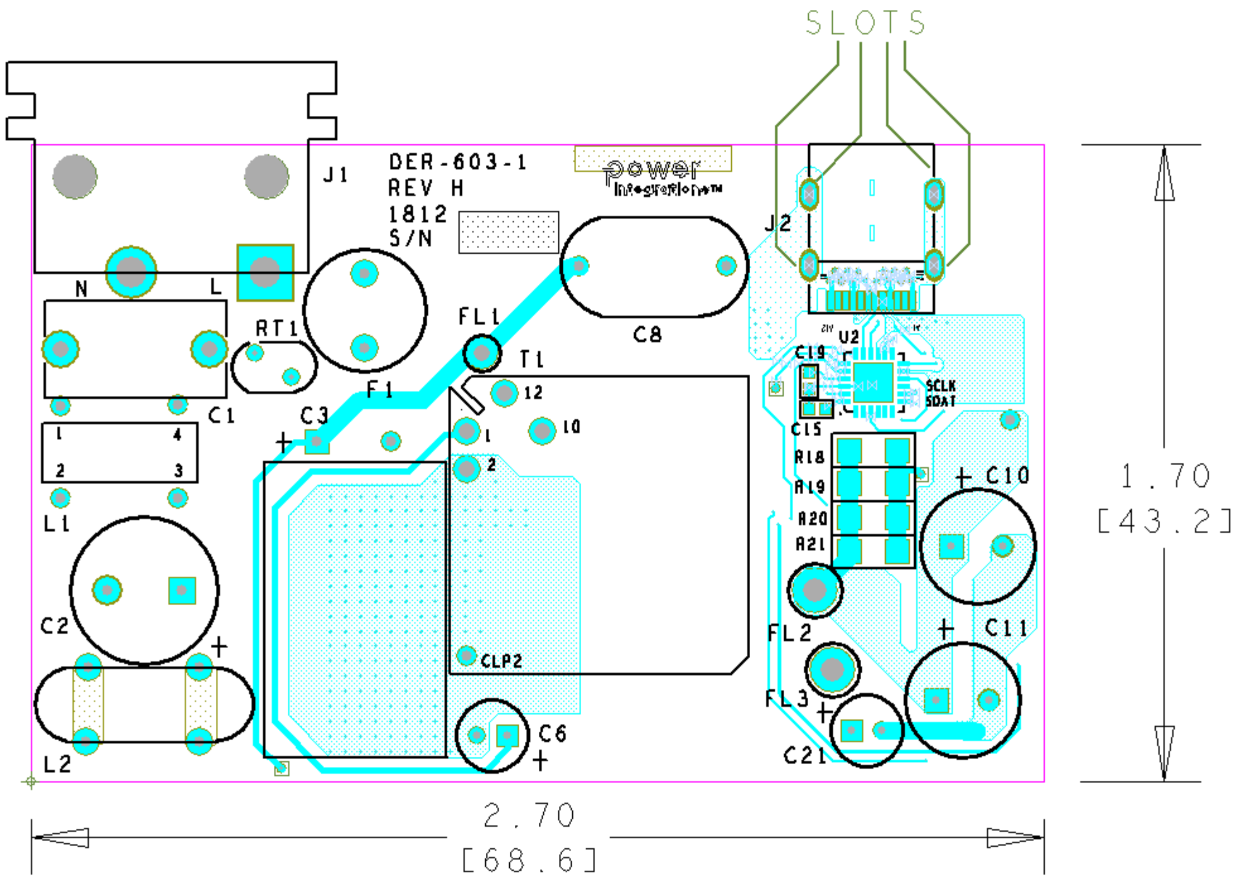

Figure 4 – Printed Circuit Layout, Top.

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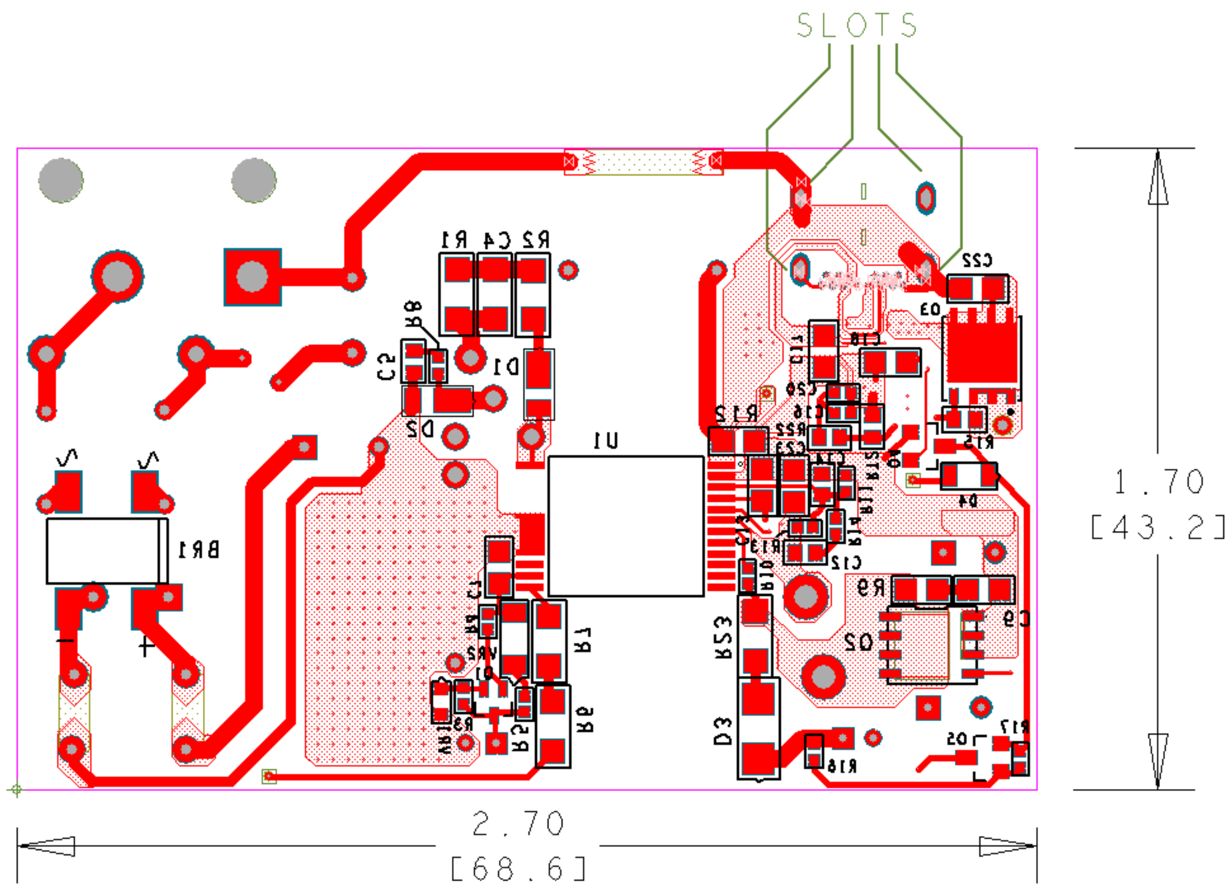

Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 2 A, Bridge Rectifier, SMD, DFS	DF206ST-G	Comchip
2	1	C1	0.1 μF, 20% , 275 VAC, 560 VDC, X2, -40°C ~ 110°C, 5 mm W x 13 mm L x 11.1 mm H	R46KF310000P1M	KEMET
3	1	C2	15 μF, 400 V, Electrolytic, (10 x 16)	UVC2G150MPD	Nichicon
4	1	C3	33 μF, 400 V, Electrolytic, (12.5 x 20)	KMG401ELL330MK20S	Nippon Chemi-Con
5	1	C4	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K	TDK
6	1	C5	56 pF, 250 V, Ceramic, NP0, 0603	GQM1875C2E560JB12D	Murata
7	1	C6	22 μF, 50 V, Electrolytic, (5 x 11)	UPW1H220MDD	Nichicon
8	1	C7	470 nF, 50 V, Ceramic, X7R, 0805	GRM21BR71H474KA88L	Murata
9	1	C8	330 pF, 250 VAC, Film, X1Y1	DE1B3KX331KN4AP01F	TDK
10	1	C9	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
11	2	C10, C11	470 μF, 16 V,Al Organic Polymer, 12 mΩ, (8 x 11.5)	RNE1C471MDN1	Nichicon
12	1	C12	4.7 nF 50 V, Ceramic, X7R, 0603	GCM188R71H472KA37D	Murata
13	2	C13, C23	2.2 μF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
14	1	C14	1000 pF, 100 V, Ceramic, NP0, 0603	C1608C0G2A102J	TDK
15	2	C15, C20	1 μF 25 V, Ceramic, X5R, 0402	TMK105BJ105MV-F	Taiyo Yuden
16	2	C16, C19	100 nF 16 V, Ceramic, X7R, 0402	L05B104KO5NNNC	Samsung
17	2	C17, C18	390 pF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB391	Yageo
18	1	C21	10 μF, 63 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG630ELL100ME11D	Nippon Chemi-Con
19	1	C22	10 μF, 16 V, Ceramic, X5R, 0805	GRM21BR61C106KE15L	Murata
20	1	D1	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
21	1	D2	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
22	1	D3	50 V, 1 A, Fast Recovery, 150 ns, SMA	RS1A-13-F	Diodes, Inc.
23	1	D4	Diode, General Purpose, Power, Switching, SS SWCH DIO, 250V, SC-76, SOD-323	BAS21HT1G	ON Semi
24	1	F1	3.15 A, 250 V, Fast, TR5	37013150410	Wickman
25	1	J1	CONN, AC Recept Panel, R/A, PCB pins	770W-X2/10	Qualtek
26	1	J2	Connector, Receptacle "Certified", USB - C, USB 3.1, For 0.062" PCB Material!, Superspeed+, 24 Position, SMT, Right Angle, Through Hole	632723300011	Wurth
27	1	L1	Toroidal Common Mode Choke, 108 μH, ±20%,primary leakage inductance = 0.5 μH, constructed on Core 35T0375-10H from PI# 30-00275-00	32-00369-00	Power Integrations
28	1	L2	Toroidal Common Mode Choke,16.6 mH,±25%, Core Effective Inductance = 5500 nH//N2, leakage inductance = 80 μH ±10%, custom, wound on 32-00286-00 core (14.90 mm O.D. 6.5 mm Th 7.0 mm ID)	32-00368-00	Power Integrations
29	1	Q1	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-323	MMST3904-7-F	Diodes, Inc.
30	1	Q2	100 V, 40 A, N-Channel, PowerPAK SO-8	SIR876ADP-T1-GE3	Vishay
31	1	Q3	MOSFET, P-CH, 30 V, 21 A, 8DFN	AON6403	Alpha & Omega Semi
32	1	Q4	MOSFET, N-CH, 60 V, 0.5 A (Ta),0.3 W (Ta) , -55°C ~ 150°C (TJ), TO-236-3, SC-59, SOT-23-3	MMBF170-7-F	Diodes, Inc.
33	1	Q5	60 V, 0.185 A, , P-Channel, SOT 23-3	TP0610K-T1-E3	Vishay
34	1	R1	RES, 205 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2053V	Panasonic
35	1	R2	RES, 14.7 Ω, 1%, 1/4 W,Thick Film, 1206	ERJ-8ENF14R7V	Panasonic
36	2	R3, R17	RES, 100 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ104X	Panasonic
37	1	R4	RES, 3.00 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3001X	Panasonic
38	1	R5	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ220X	Panasonic
39	1	R6	RES, 1.80 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
40	1	R7	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
41	1	R8	RES, 100 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ101X	Panasonic

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42	1	R9	RES, 5.6 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ5R6V	Panasonic
43	1	R10	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ470X	Panasonic
44	1	R11	RES, 68.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF6802X	Panasonic
45	1	R12	RES, 0.005 Ω, 0.5 W, 1%, 0805	PMR10EZPFU5L00	Rohm
46	1	R13	RES, 200.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF2003X	Panasonic
47	1	R14	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ102X	Panasonic
48	1	R15	RES, 1 MΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ105V	Panasonic
49	1	R16	RES, 20.5 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF2052X	Panasonic
50	2	R18, R19	RES, 158 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1580V	Panasonic
51	1	R22	RES, 100 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
52	1	R23	RES, 10 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF10R0V	Panasonic
53	1	RT1	NTC Thermistor, 5 Ω, 1 A	MF72-005D5	Cantherm
54	1	RT2	NTC Thermistor, 100 kΩ, 3%, 0603	NCP18WF104E03RB	Murata
55	1	T1	Bobbin, RM8, Vertical, 12 pins	BRM08-1112CP-W-P5.0	MH&W
56	1	U1	InnoSwitch3-CP	INN3266C-H210	Power Integrations
57	1	U2	USB Type-C Port Controller	CYPD3175-24LQXQ	Cypress
58	1	VR1	10 V, 5%, 150 mW, SSMINI-2	DZ2S100M0L	Panasonic
59	1	VR2	DIODE ZENER 30 V 500 mW SOD123	MMSZ5256B-7-F	Diodes, Inc.

Note: R20 and R21 are N.A. and have been removed from the schematic though a provision is made on the board layout.

7 Transformer Specification

7.1 Electrical Diagram

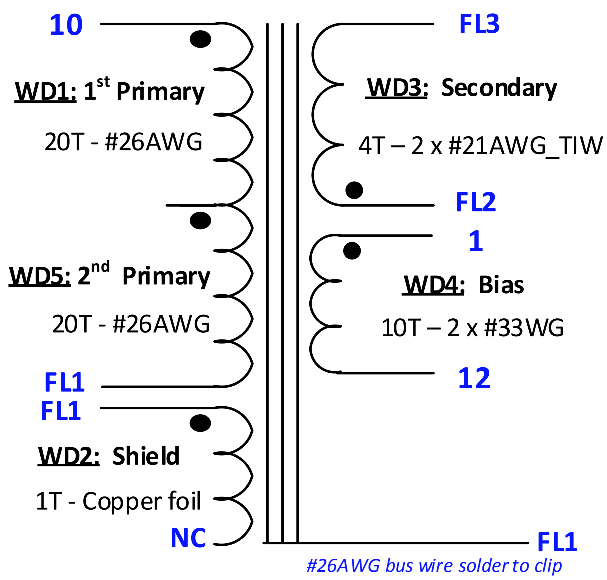

Figure 6 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	60 second, 60 Hz, from pins 10, FL1, 1, 12 to FL2 - FL3.	3000 VAC
Primary Inductance	Pins 10 - FL1, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	570 µH, ±7%
Resonant Frequency	Pins 10 - FL1, all other windings open.	1000 kHz (Min.)
Primary Leakage Inductance	Pins 10 - FL1, with FL1 - FL2 shorted, measured at 100 kHz, 0.4 V_{RMS}.	6.5 µH (Max.)

7.3 Material List

Item	Description
[1]	Core: TDK PC95-RM8.
[2]	Bobbin: RM8-V-12(6/6), circular, PI#: 25-01084-00; or equivalent. Remove all secondary pins and trim round bottom secondary flange to match with top flange.
[3]	Clip: RM8, Allstar Magnetic, CLI/P-RM8/I.
[4]	Magnet Wire: #26 AWG, Solderable Double Coated.
[5]	Magnet Wire: #33 AWG, Solderable Double Coated.
[6]	Magnet Wire: #21 AWG, Triple Insulated Wire.
[7]	Tape: Polyester Film, 3M, 1 mil thick, 9.3 mm Wide.
[8]	Tape: Polyester Film, 3M, 1 mil thick, 30.0 mm x 55.0 mm.
[9]	Copper Tape: 8.6 mm width x 37.0 mm length x 1 mil thick, soldered with magnetic wire #32 AWG at 1 end, and wrap left edge with tape. (see Figure 9 for construction).
[10]	Varnish: Dolph BC 359.

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7.4 Transformer Build Diagram

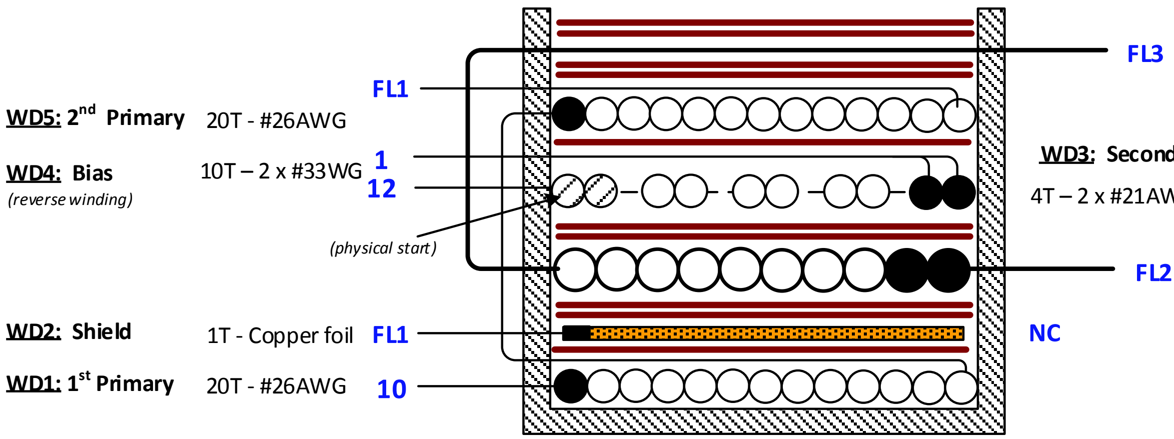

Figure 7 – Transformer Construction Diagram.

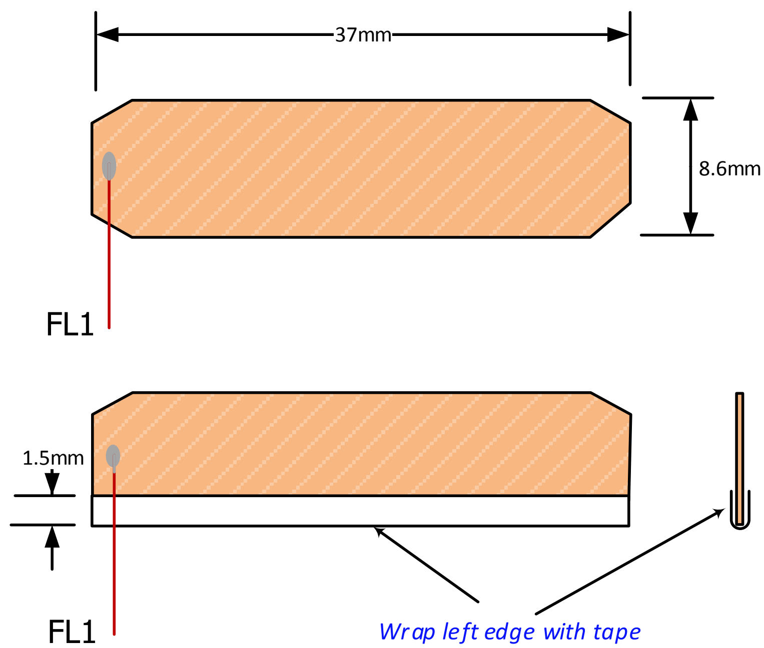

Figure 8 – Copper Shield Construction.

7.5 Winding Instruction

Winding Preparation	Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 1st Primary	Start at pin 10, wind 20 turns of wire Item [4] in 1 layer, with tight tension, from left to right. At the last turn bring the wire back to the left and leave 3ft of wire for 2nd primary winding – WD5.
Insulation	1 layer of tape Item [7].
WD2 Shield	Use copper Item [9], start as FL1 with the wire which is soldered with the copper foil, wind 1 turn overlapped but not shorted.
Insulation	2 layers of tape Item [7].
WD3 Secondary	Use 2 wires Item [6], leave ~1" floating, and mark as FL2. Start at the slot on the right of the bobbin, and wind 4 turns with tight tension in 1 layer. At the last turn, exit the wires at the slot on the left of bobbin and leave ~2" as FL3.
Insulation	2 layers of tape Item [7].
WD4 Bias	Turn the bobbin on the mandrel with secondary on the right because of reverse direction for this winding. Start at pin 12, use 2 wires Item [5], wind 10 turns in 1 layer, from right to left, spread the wires evenly across the bobbin. At the last turn bring the wires back to the right and finish at pin 1.
Insulation	1 layer of tape Item [7].
WD5 2nd Primary	Now turn bobbin back to normal position, continue winding 20 turns with the wire floating for WD1. At the last turn, leave ~ 1" floating and also mark as FL1.
Finish	Apply 2 layers of tape Item [7], bring wires floating FL3 from WD3-Secondary to the right and continue to apply 2 layers of tape to secure all windings. Gap core halves to 570 μH, secure with clips Item [3] with GND pins on top and cut short. Varnish with Item [10]. Place 2 layers of tape Item [8] at the bottom of transformer then wrap up to body of transformer, and wrap around transformer with 1 turn of tape Item [7]. Solder bus wire #26 AWG to 1 clip and also mark as FL1.

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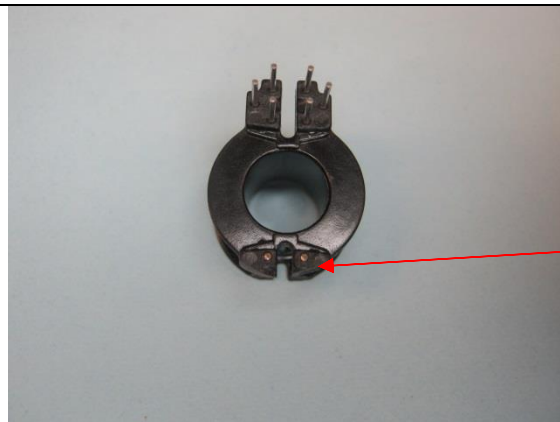
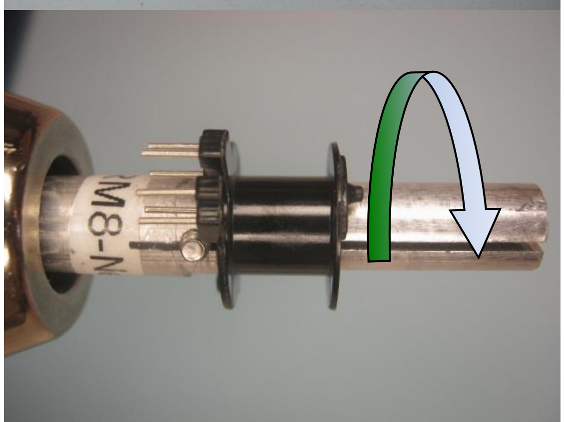
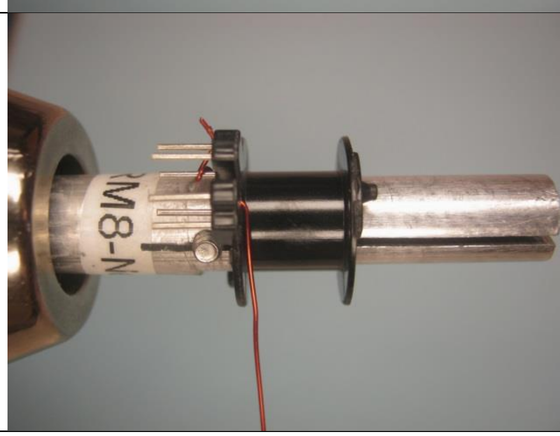
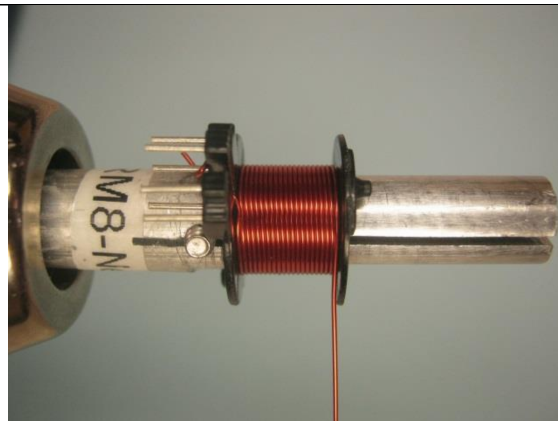
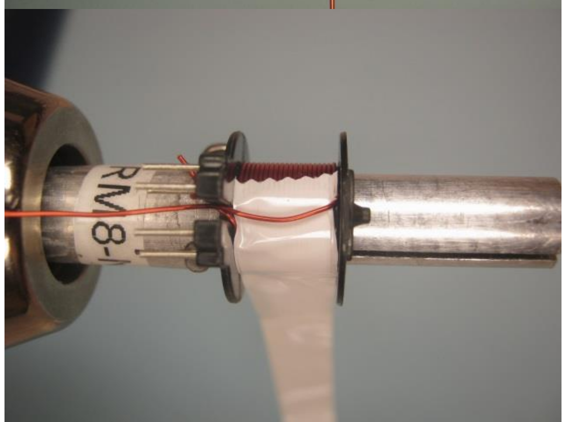
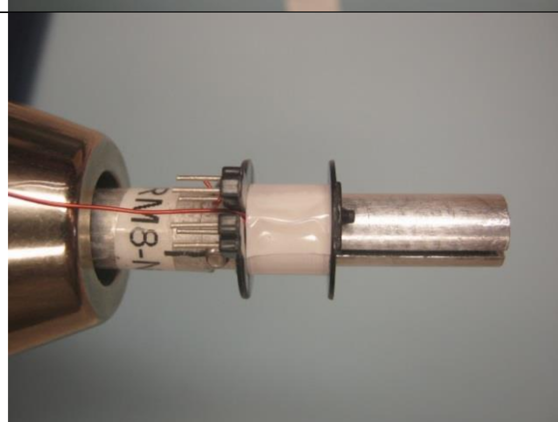
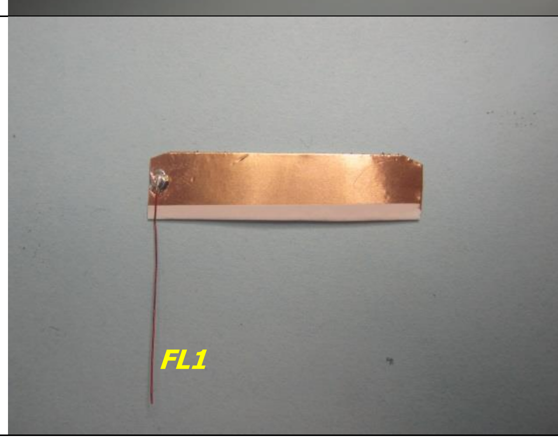
7.6 Winding Illustration

Winding preparation	 	All secondary pins to be removed from the bobbin and the secondary flange should be trimmed such that the round bottom matches with the top flange. Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 **1st Primary**		Start at pin 10, wind 20 turns of wire Item [4] in 1 layer, with tight tension, from left to right. At the last turn bring the wire back to the left and leave 3ft of wire for 2nd primary winding – WD5.

	 	
Insulation		1 layer of tape Item [7].
		Prepare copper foil Item [9] as shown in Figure 8

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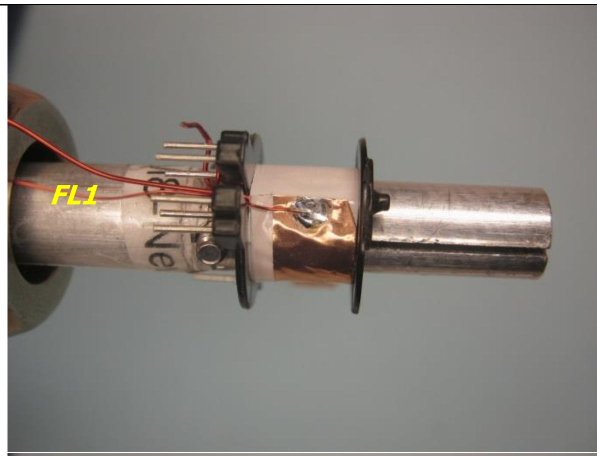
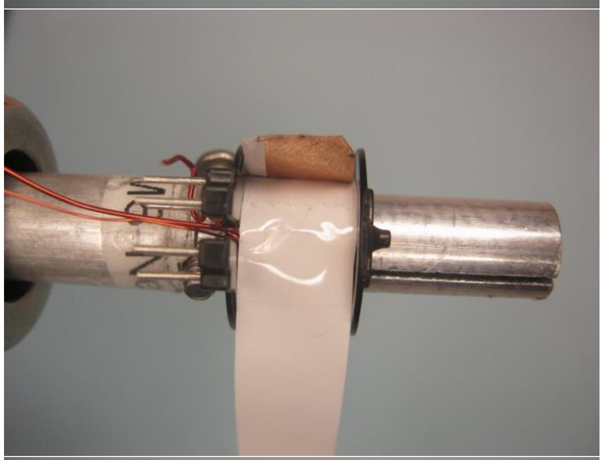
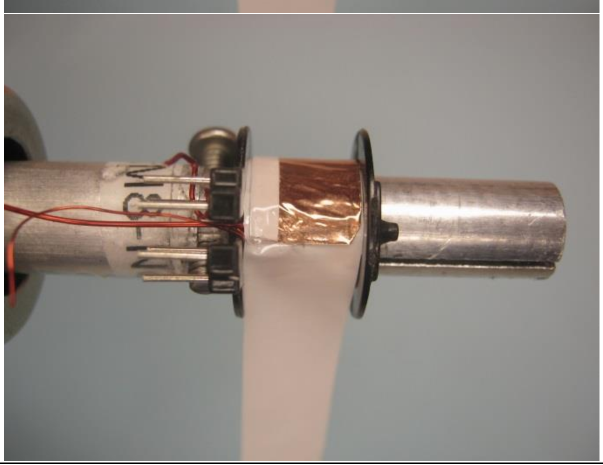
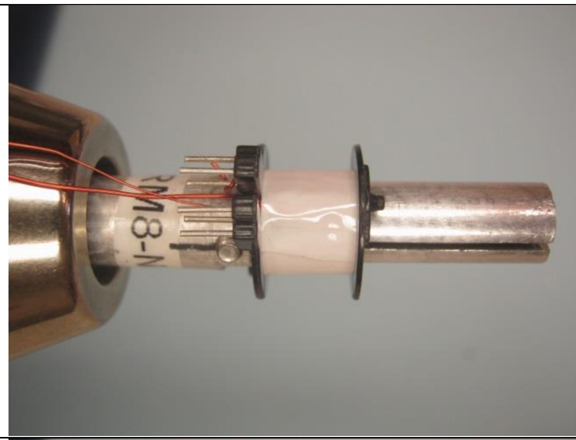
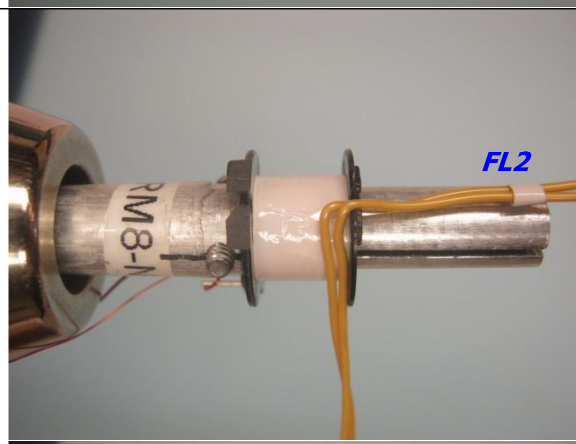
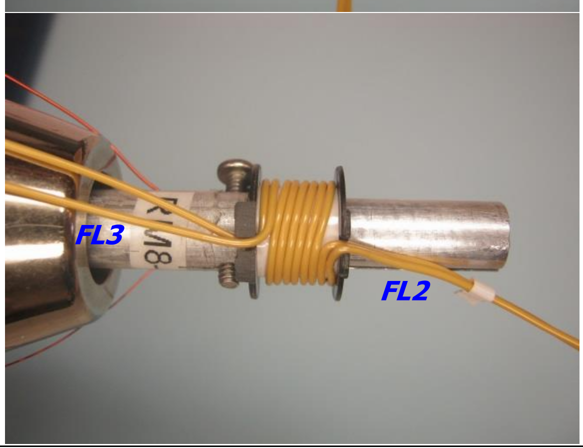
WD2 **Shield**		Start winding the copper foil from the end with FL1 wire connected. Wind 1 turn overlapped but not shorted.

Insulation		2 layers of tape Item [7].
WD3 **Secondary**		Use 2 wires Item [6], leave ~1” floating, and mark as FL2. Start at the slot on the right of the bobbin, and wind 4 turns with tight tension in 1 layer. At the last turn, exit the wires at the slot on the left of bobbin and leave ~2” as FL3.

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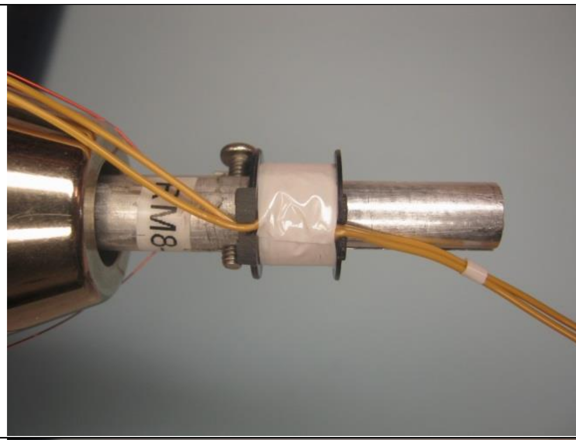
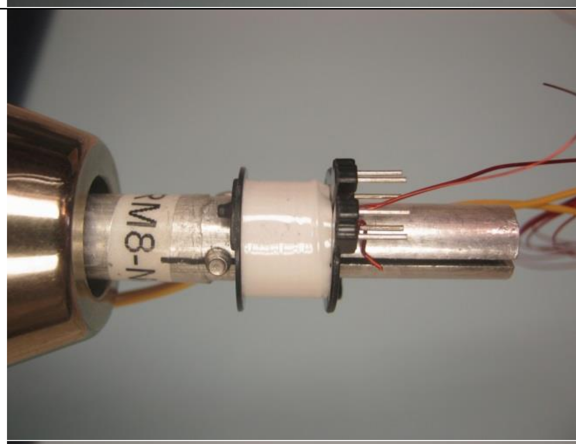
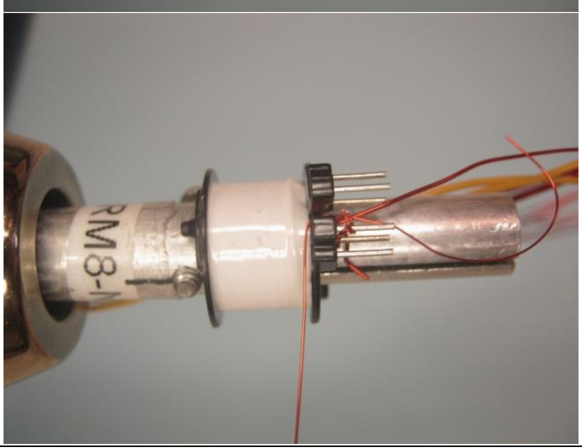
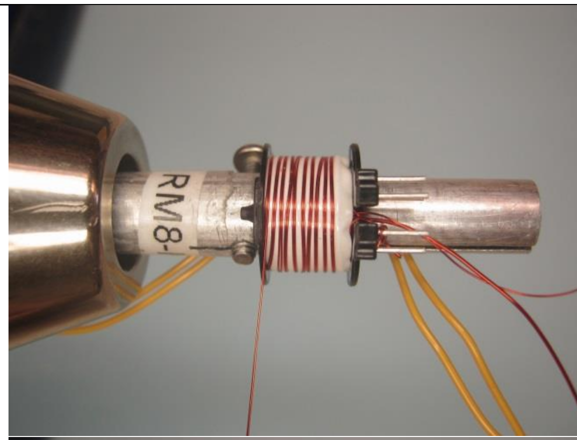
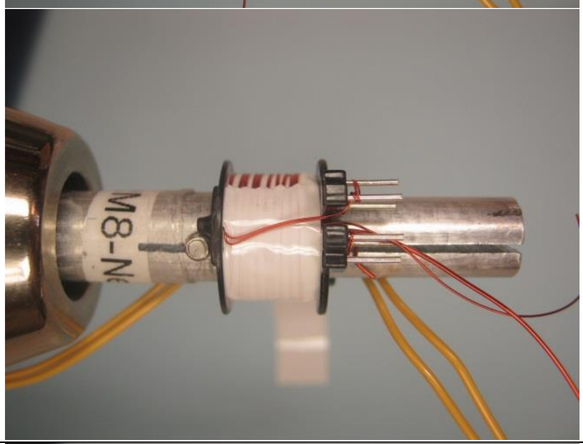
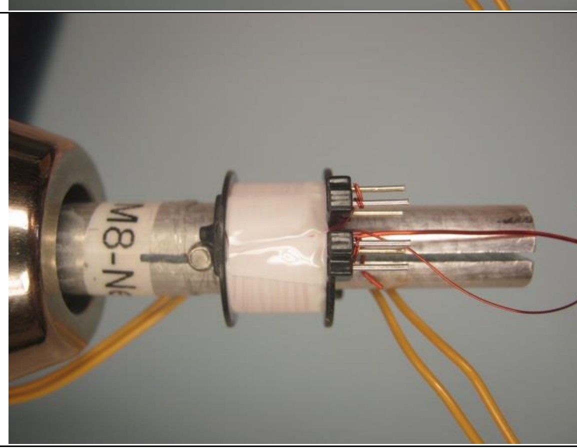
Insulation		2 layers of tape Item [7].
WD4 **Bias**	 	Turn the bobbin on the mandrel with secondary on the right because of reverse direction for this winding. Start at pin 12, use 2 wires of Item [5], wind 10 turns in 1 layer, from right to left, spread the wires evenly across the bobbin. At the last turn bring the wires back to the right and finish at pin 1.

	 	
Insulation		1 layer of tape Item [7].

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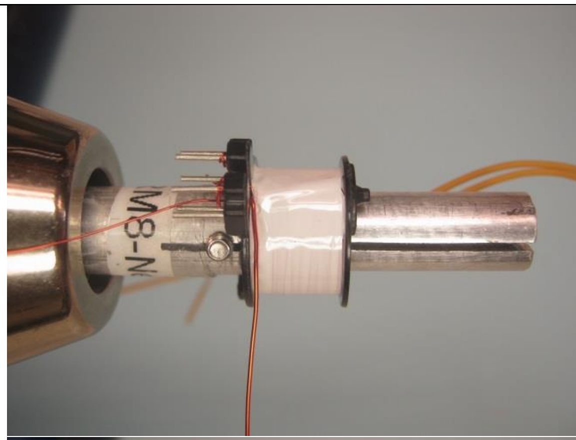
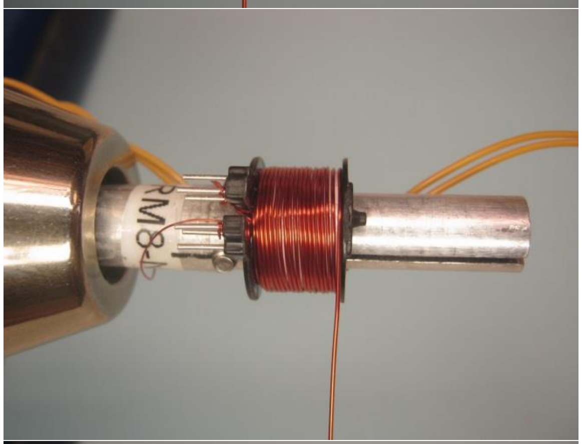
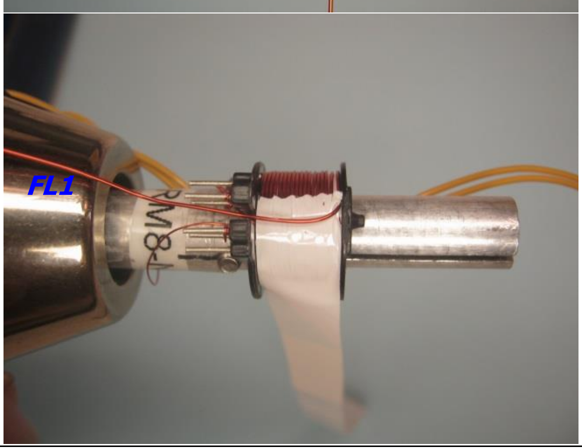
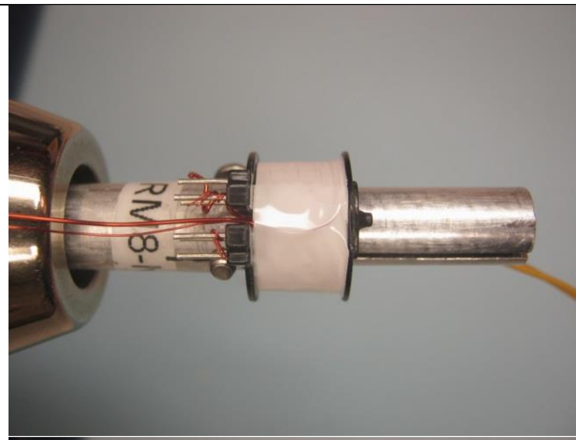
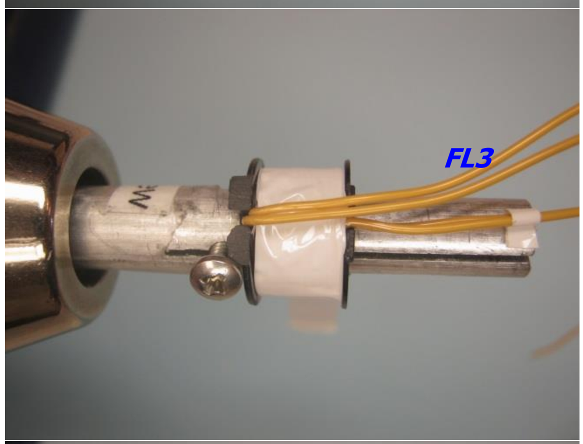
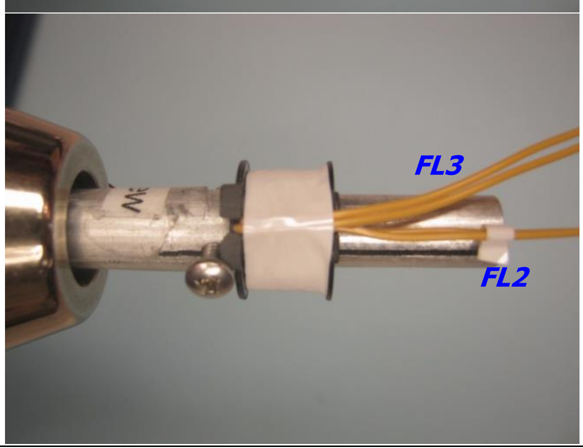
WD5 **2nd Primary**	   	Now turn bobbin back to normal position, continue winding 20 turns with the wire floating for WD1. At the last turn, leave the ~1" floating and also mark as FL1.

Finish	   	Apply 2 layers of tape Item [7], bring floating wires FL3 from WD3-Secondary to the right and continue to apply 2 layers of tape to secure all windings. Gap core halves to 570 μH, secure with clips- Item [3] with GND pins on top and cut short. Varnish with Item [10]. Place 2 layers of tape Item [8] at the bottom of transformer then wrap up to body of transformer, and wrap around transformer with 1 turn of tape Item [7]. Solder bus wire #26 AWG to 1 clip and also mark as FL1.

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	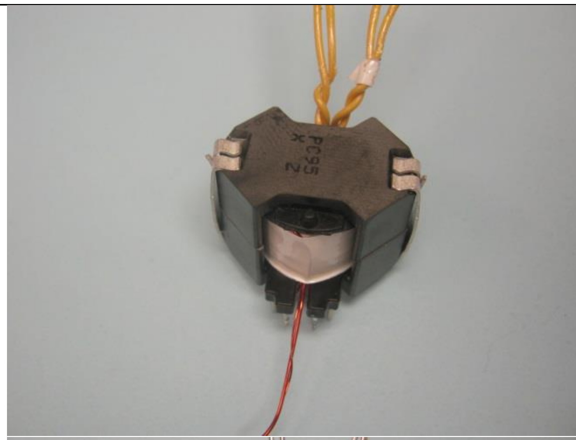 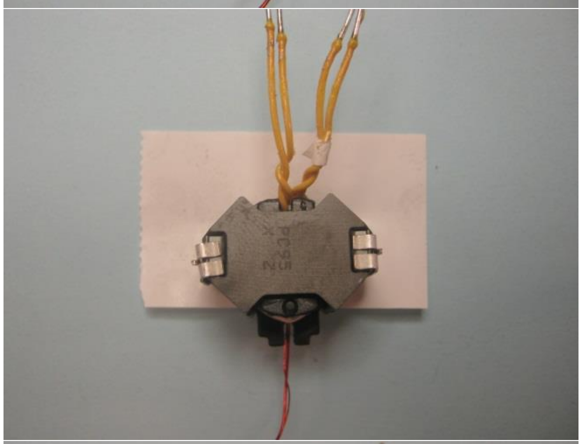 	

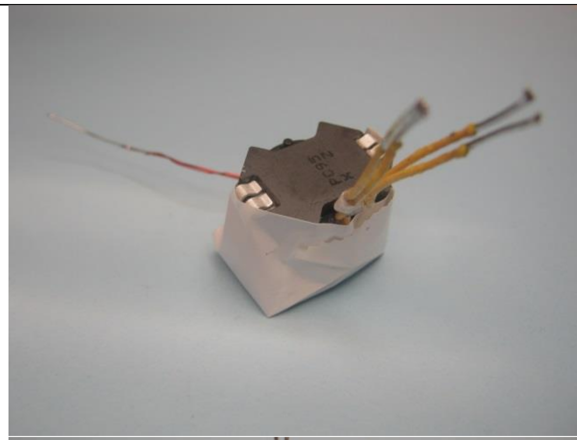

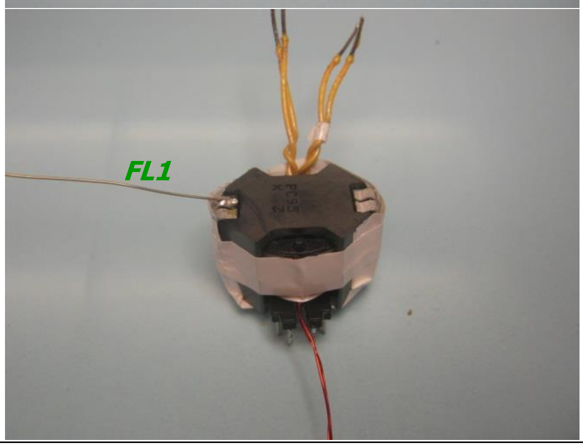

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8 Common Mode Choke Specifications

8.1 108 μH Common Mode Choke (L1)

8.1.1 *Electrical Diagram*

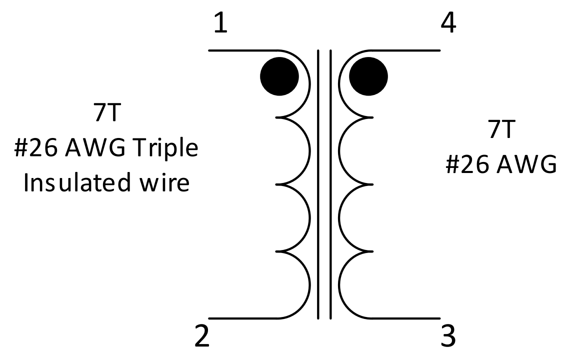

Figure 9 – Inductor Electrical Diagram.

8.1.2 *Electrical Specifications*

Inductance	Pins 1-2 measured at 100 kHz, 0.4 RMS.	108 μH ±20%
Primary Leakage Inductance	Pins 1-2, with 3-4 shorted.	0.5 μH

8.1.3 *Material List*

Item	Description
[1]	Toroid: FERRITE INDUCTR TOROID .415" O.D.;Mfg Part number: 35T0375-10H. Dim: 9.53 mm O.D. x 4.75 mm I.D. x 3.18 mm L.
[2]	Magnet Wire: #26 AWG.
[3]	Triple Insulated Wire #26 AWG.

8.1.4 *Illustration*

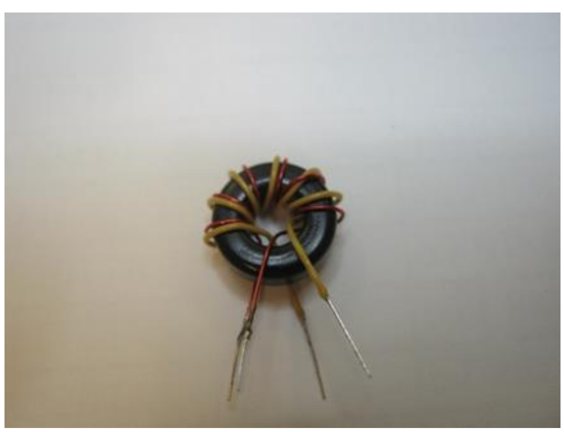

Figure 10 – L1 Front View.

8.2 16.6 mH Common Mode Choke (L3)

8.2.1 *Electrical Diagram*

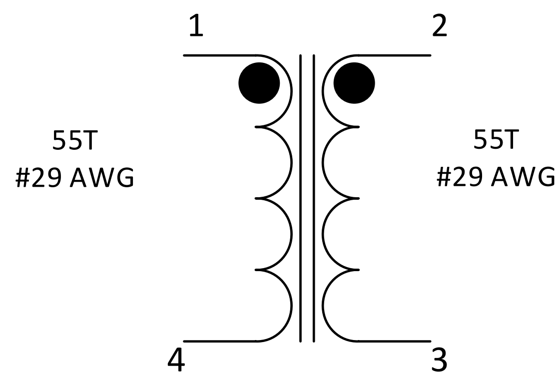

Figure 12 – Inductor Electrical Diagram.

8.2.2 *Electrical Specifications*

Inductance	Pins 1-4 and pins 2-3 measured at 100 kHz, 0.4 RMS.	16.6 mH ±25%
Core effective Inductance		5500 nH/N^2
Primary Leakage Inductance	Pins 1-4, with 2-3 shorted.	80 μH

8.2.3 *Materials List*

Item	Description
[1]	Toroid: FERRITE INDUCTR TOROID T14 x 8 x 5.5, PI#: 32-00286-00.
[2]	Divider: Cable Tie, Panduit -- Fish Paper, Insulating Cotton Rag, 0.010” thick, PI #: 66-00042-00
[3]	Magnet Wire: #29 AWG Heavy Nyleze.
[4]	Epoxy: Devon, 5 mins Epoxy; or Equivalent.

8.2.4 *Winding Instructions*

- Place 2 pieces of cable tie Item [2] on to toroid Item [1] to divide 2 equal sections.
- Use 4 ft of wire Item [3], start as 1, wind 55 turns in 2 layers in 1 section of toroid, and end as 4.
- Do the same for another half of Toroid, start as 2 and end as 3.
- Pull up 2 notches of cable ties to be in line with toroid body (to save space), and apply Epoxy Item [4] where leads floating.

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8.2.5 *Illustration*

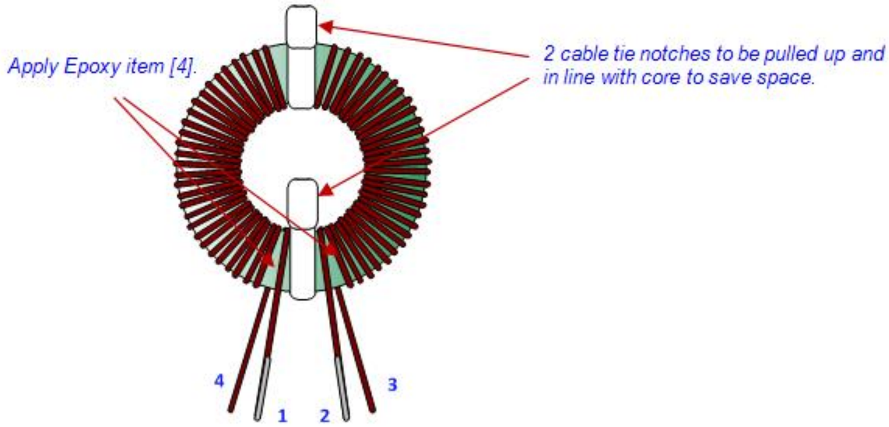

Figure 13 – Side View.

9 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-CP_Flyback_022018; Rev.1.2; Copyright Power Integrations 2018	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-CP Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VAC_MIN			85	V	Minimum AC line voltage
4	VAC_MAX			265	V	Maximum AC input voltage
5	VAC_RANGE			UNIVERSAL		AC line voltage range
6	FLINE			60	Hz	AC line voltage frequency
7	CAP_INPUT	48.0		48.0	uF	Input capacitance
9	**SETPOINT 1**					
10	VOUT1	11.00		11.00	V	Output voltage 1, should be the highest output voltage required
11	IOUT1	2.450		2.450	A	Output current 1
12	POUT1			26.95	W	Output power 1
13	EFFICIENCY1	0.87		0.87		Converter efficiency for output 1
14	Z_FACTOR1	0.50		0.50		Z-factor for output 1
16	**SETPOINT 2**					
17	VOUT2	9.00		9.00	V	Output voltage 2
18	IOUT2	3.000		3.000	A	Output current 2
19	POUT2			27.00	W	Output power 2
20	EFFICIENCY2	0.86		0.86		Converter efficiency for output 2
21	Z_FACTOR2	0.50		0.50		Z-factor for output 2
23	**SETPOINT 3**					
24	VOUT3	5.00		5.00	V	Output voltage 3
25	IOUT3	3.000		3.000	A	Output current 3
26	POUT3			15.00	W	Output power 3
27	EFFICIENCY3	0.87		0.87		Converter efficiency for output 3
28	Z_FACTOR3	0.50		0.50		Z-factor for output 3
30	**SETPOINT 4**					
31	VOUT4	3.00		3.00	V	Output voltage 4
32	IOUT4	3.000		3.000	A	Output current 4
33	POUT4			9.00	W	Output power 4
34	EFFICIENCY4	0.84		0.84		Converter efficiency for output 4
35	Z_FACTOR4	0.50		0.50		Z-factor for output 4
37	**SETPOINT 5**					
38	VOUT5			0.00	V	Output voltage 5
39	IOUT5			0.000	A	Output current 5
40	POUT5			0.00	W	Output power 5
41	EFFICIENCY5			0.00		Converter efficiency for output 5
42	Z_FACTOR5			0.00		Z-factor for output 5
44	**SETPOINT 6**					
45	VOUT6			0.00	V	Output voltage 6
46	IOUT6			0.000	A	Output current 6
47	POUT6			0.00	W	Output power 6
48	EFFICIENCY6			0.00		Converter efficiency for output 6
49	Z_FACTOR6			0.00		Z-factor for output 6
51	**SETPOINT 7**					
52	VOUT7			0.00	V	Output voltage 7
53	IOUT7			0.000	A	Output current 7
54	POUT7			0.00	W	Output power 7
55	EFFICIENCY7			0.00		Converter efficiency for output 7
56	Z_FACTOR7			0.00		Z-factor for output 7
58	**SETPOINT 8**					
59	VOUT8			0.00	V	Output voltage 8
60	IOUT8			0.000	A	Output current 8
61	POUT8			0.00	W	Output power 8
62	EFFICIENCY8			0.00		Converter efficiency for output 8
63	Z_FACTOR8			0.00		Z-factor for output 8

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65	**SETPOINT 9**					
66	VOUT9			0.00	V	Output voltage 9
67	IOUT9			0.000	A	Output current 9
68	POUT9			0.00	W	Output power 9
69	EFFICIENCY9			0.00		Converter efficiency for output 9
70	Z_FACTOR9			0.00		Z-factor for output 9
71						
72	PERCENT_CDC	0%		0%		Percentage (of output voltage) cable drop compensation desired at full load
73	CDC_SCALING_SETPOINT	3		3		Select the setpoint number for the voltage used for cable drop compensation (typically the 5V output)
77	**PRIMARY CONTROLLER SELECTION**					
78	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
79	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
80	VDRAIN_BREAKDOWN	650		650	V	Device breakdown voltage
81	DEVICE_GENERIC	INN32X6		INN32X6		Device selection
82	DEVICE_CODE			INN3266C		Device code
83	PDEVICE_MAX			27	W	Device maximum power capability
84	RDSON_25DEG			1.50	Ω	Primary MOSFET on-time resistance at 25°C
85	RDSON_100DEG			2.32	Ω	Primary MOSFET on-time resistance at 100°C
86	ILIMIT_MIN			1.162	A	Primary MOSFET minimum current limit
87	ILIMIT_TYP			1.250	A	Primary MOSFET typical current limit
88	ILIMIT_MAX			1.338	A	Primary MOSFET maximum current limit
89	VDRAIN_ON_MOSFET			0.85	V	Primary MOSFET on-time voltage drop
90	VDRAIN_OFF_MOSFET			553.31	V	Peak drain voltage on the primary MOSFET during turn-off
94	**WORST CASE ELECTRICAL PARAMETERS**					
95	FSWITCHING_MAX	87477		87477	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
96	VOR	110.0		110.0	V	Voltage reflected to the primary winding (corresponding to setpoint 1) when the primary MOSFET turns off
97	VMIN			80.44	V	Valley of the rectified minimum input AC voltage at full load
98	KP			0.780		Measure of continuous/discontinuous mode of operation
99	MODE_OPERATION			CCM		Mode of operation
100	DUTYCYCLE			0.579		Primary MOSFET duty cycle
101	TIME_ON			9.55	us	Primary MOSFET on-time
102	TIME_OFF			4.99	us	Primary MOSFET off-time
103	LPRIMARY_MIN			530.1	uH	Minimum primary magnetizing inductance
104	LPRIMARY_TYP			570.0	uH	Typical primary magnetizing inductance
105	LPRIMARY_TOL	7.0		7.0		Primary magnetizing inductance tolerance
106	LPRIMARY_MAX			609.9	uH	Maximum primary magnetizing inductance
108	**PRIMARY CURRENT**					
109	IAVG_PRIMARY			0.367	A	Primary MOSFET average current
110	IPEAK_PRIMARY			1.278	A	Primary MOSFET peak current
111	IPEDESTAL_PRIMARY			0.249	A	Primary MOSFET current pedestal
112	IRIPPLE_PRIMARY			1.276	A	Primary MOSFET ripple current
113	IRMS_PRIMARY			0.561	A	Primary MOSFET RMS current
115	**SECONDARY CURRENT**					
116	IPEAK_SECONDARY			12.779	A	Secondary MOSFET peak current
117	IPEDESTAL_SECONDARY			2.492	A	Secondary MOSFET pedestal current
118	IRMS_SECONDARY			5.268	A	Secondary MOSFET RMS current
119	IRIPPLE_CAP_OUT			4.330	A	Output capacitor ripple current
123	**TRANSFORMER CONSTRUCTION PARAMETERS**					
124	**CORE SELECTION**					

125	CORE	RM8	Info	RM8		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
126	CORE NAME			PC95RM08Z		Core code
127	AE			64.0	mm^2	Core cross sectional area
128	LE			38.0	mm	Core magnetic path length
129	AL			5290	nH	Ungapped core effective inductance per turns squared
130	VE			2430	mm^3	Core volume
131	BOBBIN NAME			B-RM08-V		Bobbin name
132	AW			30.0	mm^2	Bobbin window area
133	BW			8.80	mm	Bobbin width
134	MARGIN			0.0	mm	Bobbin safety margin
136	**PRIMARY WINDING**					
137	NPRIMARY			40		Primary winding number of turns
138	BPEAK			3263	Gauss	Peak flux density
139	BMAX			2995	Gauss	Maximum flux density
140	BAC			1494	Gauss	AC flux density (0.5 x Peak to Peak)
141	ALG			356	nH	Typical gapped core effective inductance per turns squared
142	LG			0.211	mm	Core gap length
143	LAYERS_PRIMARY			2		Primary winding number of layers
144	AWG_PRIMARY	26		26		Primary wire gauge
145	OD_PRIMARY_INSULATED			0.465	mm	Primary wire insulated outer diameter
146	OD_PRIMARY_BARE			0.405	mm	Primary wire bare outer diameter
147	CMA_PRIMARY			453.2	Cmils/A	Primary winding wire CMA
149	**SECONDARY WINDING**					
150	NSECONDARY	4		4		Secondary winding number of turns
151	AWG_SECONDARY			19		Secondary wire gauge
152	OD_SECONDARY_INSULATED			1.217	mm	Secondary wire insulated outer diameter
153	OD_SECONDARY_BARE			0.912		Secondary wire bare outer diameter
154	CMA_SECONDARY			244.5	Cmils/A	Secondary winding wire CMA
156	**BIAS WINDING**					
157	NBIAS			10		Bias winding number of turns
161	**PRIMARY COMPONENTS SELECTION**					
162	**LINE UNDERVOLTAGE**					
163	BROWN-IN REQURED	76.00		76.00	V	Required line brown-in threshold
164	RLS			3.82	MΩ	Connect two 1.91 MOhm resistors to the V-pin for the required UV/OV threshold
165	BROWN-IN ACTUAL			76.58	V	Actual brown-in threshold using standard resistors
166	BROWN-OUT ACTUAL			69.26	V	Actual brown-out threshold using standard resistors
168	**LINE OVERVOLTAGE**					
169	OVERVOLTAGE_LINE		Warning	319.20	V	The device voltage stress will be higher than 90% of the breakdown voltage when overvoltage is trigerred
171	**BIAS WINDING**					
172	VBIAS	7.00	Info	7.00	V	The rectified bias voltage maybe too low to supply the BP pin: Increase the rectified bias voltage to a value higher than 9V
173	VF_BIAS			0.70	V	Bias winding diode forward drop
174	VREVERSE_BIASDIODE			100.33	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
175	CBIAS			22	uF	Bias winding rectification capacitor
176	CBPP			0.47	uF	BPP pin capacitor
180	**SECONDARY COMPONENTS SELECTION**					
181	**RECTIFIER**					
182	VDRAIN_OFF_SRFET			48.33	V	Secondary rectifier reverse voltage (not

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						accounting parasitic voltage ring)
183	SRFET	SiR876ADP		SiR876ADP		Secondary rectifier (Logic MOSFET)
184	VBREAKDOWN_SRFET			100	V	Secondary rectifier breakdown voltage
185	RDSON_SRFET			14.5	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
187	**FEEDBACK COMPONENTS**					
188	RFB_UPPER	200.00		200.00	kΩ	Upper feedback resistor (connected to the output terminal)
189	RFB_LOWER			68.10	kΩ	Lower feedback resistor required to obtain the output for cable drop compensation
190	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
194	**VARIABLE OUTPUTS ANALYSIS**					
195	**TOLERANCE CORNER**					
196	CORNER_VAC			85	V	Input AC RMS voltage corner to be evaluated
197	CORNER_ILIMIT	TYP		1.250	A	Current limit corner to be evaluated
198	CORNER_LPRIMARY	TYP		570.0	uH	Primary inductance corner to be evaluated
200	**SETPOINT SELECTION**					
201	SETPOINT	1		1		Select the setpoint which needs to be evaluated
202	FSWITCHING			70614.2	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
203	VOR			110.0	V	Voltage reflected to the primary winding when the primary MOSFET turns off
204	VMIN			80.98	V	Valley of the minimum input AC voltage
205	KP			0.959		Measure of continuous/discontinuous mode of operation
206	MODE_OPERATION			CCM		Mode of operation
207	DUTYCYCLE			0.579		Primary MOSFET duty cycle
208	TIME_ON			8.19	us	Primary controller's maximum on-time
209	TIME_OFF			5.97	us	Primary controller's minimum off-time
211	**PRIMARY CURRENT**					
212	IAVG_PRIMARY			0.361	A	Primary MOSFET average current
213	IPEAK_PRIMARY			1.201	A	Primary MOSFET peak current
214	IPEDESTAL_PRIMARY			0.049	A	Primary MOSFET current pedestal
215	IRIPPLE_PRIMARY			1.152	A	Primary MOSFET ripple current
216	IRMS_PRIMARY			0.538	A	Primary MOSFET RMS current
218	**SECONDARY CURRENT**					
219	IPEAK_SECONDARY			12.006	A	Secondary MOSFET peak current
220	IPEDESTAL_SECONDARY			0.488	A	Secondary MOSFET pedestal current
221	IRMS_SECONDARY			4.594	A	Secondary MOSFET RMS current
222	IRIPPLE_CAP_OUT			3.887	A	Output capacitor ripple current
224	**MAGNETIC FLUX DENSITY**					
225	BPEAK			2849	Gauss	Peak flux density
226	BMAX			2673	Gauss	Maximum flux density
227	BAC			1282	Gauss	AC flux density (0.5 x Peak to Peak)

Note 1: The upper feedback divider resistor is 200 kΩ and lower feedback divider resistor is 68 kΩ in order to meet CCG3PA requirements.

Note 2: The OVERVOLTAGE_LINE shows a warning. Calculations and test data show that this voltage is within the limits and there is sufficient margin hence this warning can be ignored.

10 Performance Data

10.1 No-Load Input Power at 5 VOUT

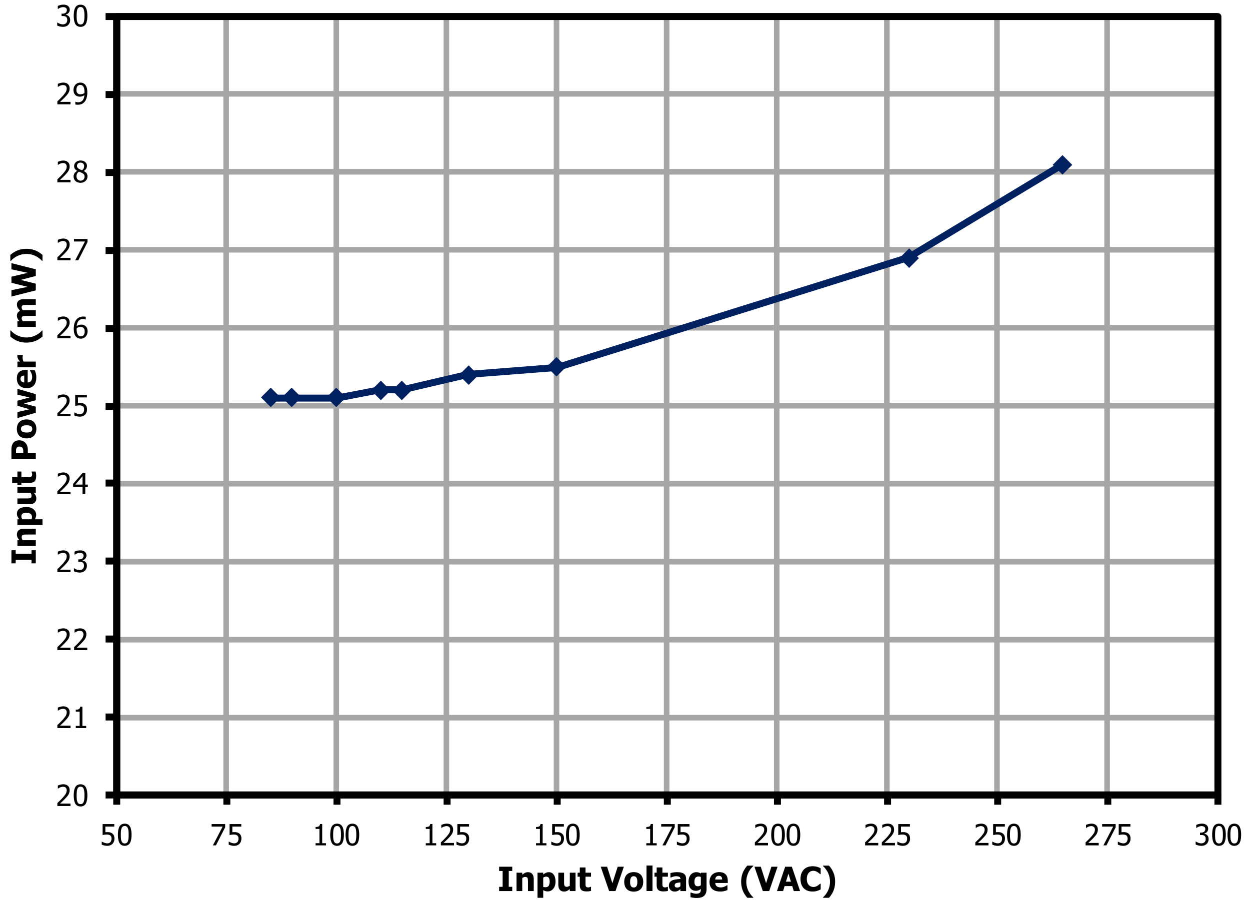

Figure 14 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

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10.2 Average Efficiency (On the Board)

10.2.1 *Average Efficiency Requirements*

Test	Power (W)	Average	Average	10% Load	Average	Average	10% Load
Model		<6 V Voltage	<6 V Voltage	<6 V Voltage	>6 V Voltage	>6 V Voltage	>6 V Voltage
Regulation		**New IESA2007**	**CoC v5 Tier 2**	**CoC v5 Tier 2**	**New IESA2007**	**CoC v5 Tier 2**	**CoC v5 Tier 2**
	9	**78%**	**78.2%**	**69%**			
	15	**81.4 %**	**81.8%**	**72.5%**			
	27				**86.6%**	**87.3%**	**77.3%**

10.3 Average Efficiency and Efficiency at 10% Load at 115 VAC Input (On the Board)

10.3.1 *5.0 V, 3 A Output*

% Load	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	Efficiency (%)	Average Efficiency (%)
100	5.01	3.01	17.03	88.60	
75	5.03	2.26	12.79	88.88	
50	5.04	1.51	8.53	89.29	
25	5.02	0.76	4.30	89.12	88.97
10	5.00	0.31	1.80	87.04	

10.3.2 *9.0 V, 3 A Output*

% Load	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	Efficiency (%)	Average Efficiency (%)
100	9.08	3.03	30.69	89.54	
75	9.11	2.28	23.10	89.80	
50	9.13	1.53	15.54	89.80	
25	9.13	0.78	7.98	89.13	89.57
10	9.11	0.33	3.51	85.65	

10.3.3 *11.0 V, 2.45 A Output*

% Load	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	Efficiency (%)	Average Efficiency (%)
100	11.11	2.48	30.66	89.94	
75	11.14	1.87	23.21	89.85	
50	11.16	1.26	15.64	89.79	
25	11.16	0.65	8.14	88.69	89.57
10	11.14	0.28	3.74	83.40	

10.3.4 *3.0 V, 3 A Output*

% Load	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	Efficiency (%)	Average Efficiency (%)
100	3.03	2.91	10.42	84.61	
75	3.04	2.18	7.85	84.36	
50	3.05	1.46	5.27	84.30	
25	3.03	0.73	2.71	82.00	83.82
10	3.02	0.30	1.21	74.33	

10.4 Average Efficiency and Efficiency at 10% Load at 230 VAC Input (On the Board)

10.4.1 *5.0 V, 3 A Output*

% Load	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	Efficiency (%)	Average Efficiency (%)
100	5.05	3.01	17.12	88.73	
75	5.05	2.26	12.80	89.19	
50	5.05	1.51	8.59	88.85	
25	5.02	0.76	4.37	87.59	88.59
10	5.01	0.31	1.87	83.61	

10.4.2 *9.0 V, 3 A Output*

% Load	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	Efficiency (%)	Average Efficiency (%)
100	9.13	3.02	30.56	90.28	
75	9.14	2.28	23.03	90.37	
50	9.15	1.53	15.53	89.97	
25	9.14	0.78	8.04	88.50	89.78
10	9.11	0.33	3.58	83.72	

10.4.3 *11.0 V, 2.45 A Output*

% Load	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	Efficiency (%)	Average Efficiency (%)
100	11.15	2.48	30.55	90.62	
75	11.16	1.87	23.09	90.43	
50	11.17	1.26	15.63	89.90	
25	11.17	0.65	8.20	88.19	89.79
10	11.14	0.28	3.77	82.85	

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10.4.4 *3.0 V, 3 A Output*

% Load	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	Efficiency (%)	Average Efficiency (%)
100	3.06	2.91	10.60	83.84	
75	3.06	2.19	8.03	83.54	
50	3.06	1.46	5.43	82.21	
25	3.03	0.73	2.84	78.37	81.99
10	3.04	0.30	1.31	69.09	

10.5 **Efficiency (On the Board)**

10.5.1 *5.0 V Output*

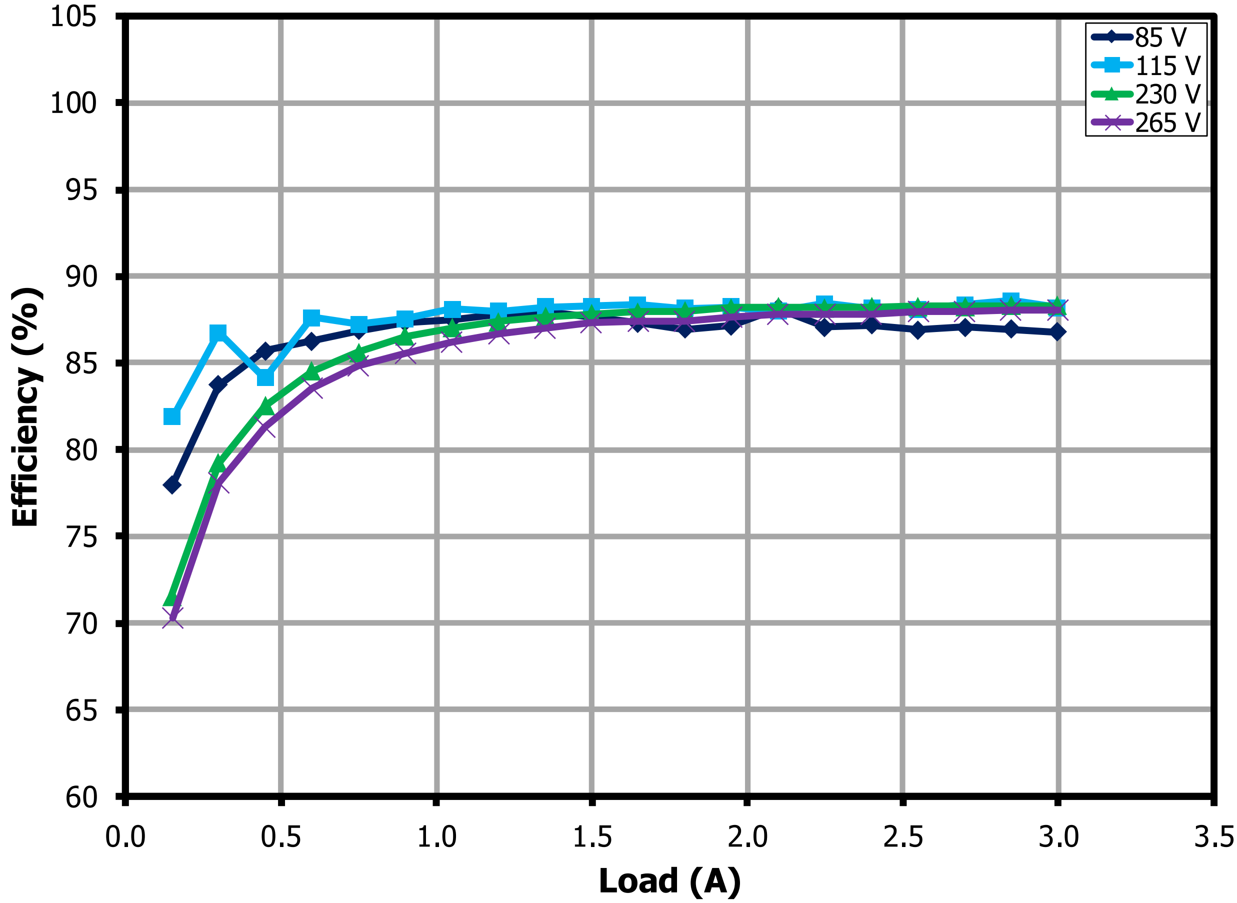

Figure 15 – Efficiency Over Line and Load for 5 V Output.

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10.5.2 *9.0 V Output*

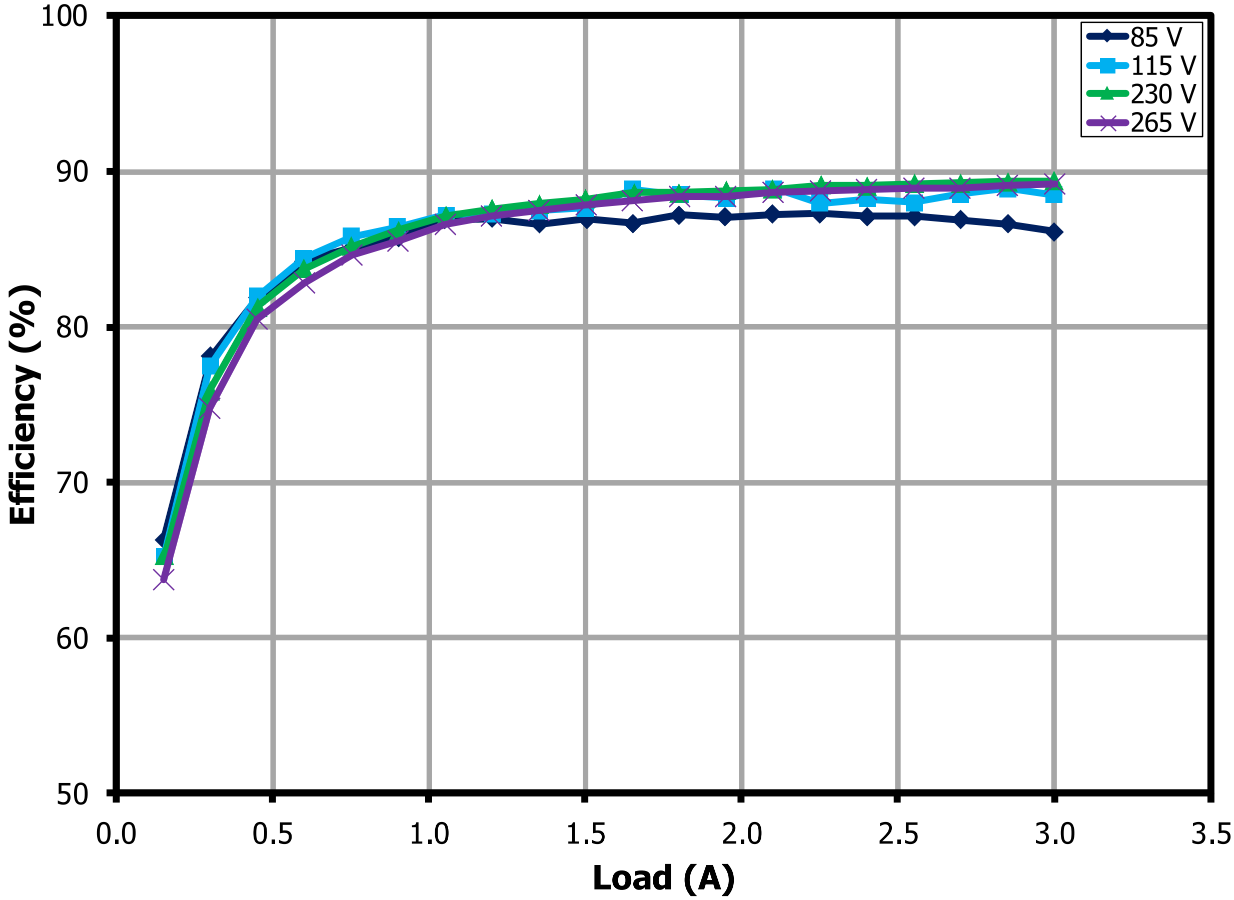

Figure 16 – Efficiency Over Line and Load for 9 V Output.

10.5.3 *11.0 V Output*

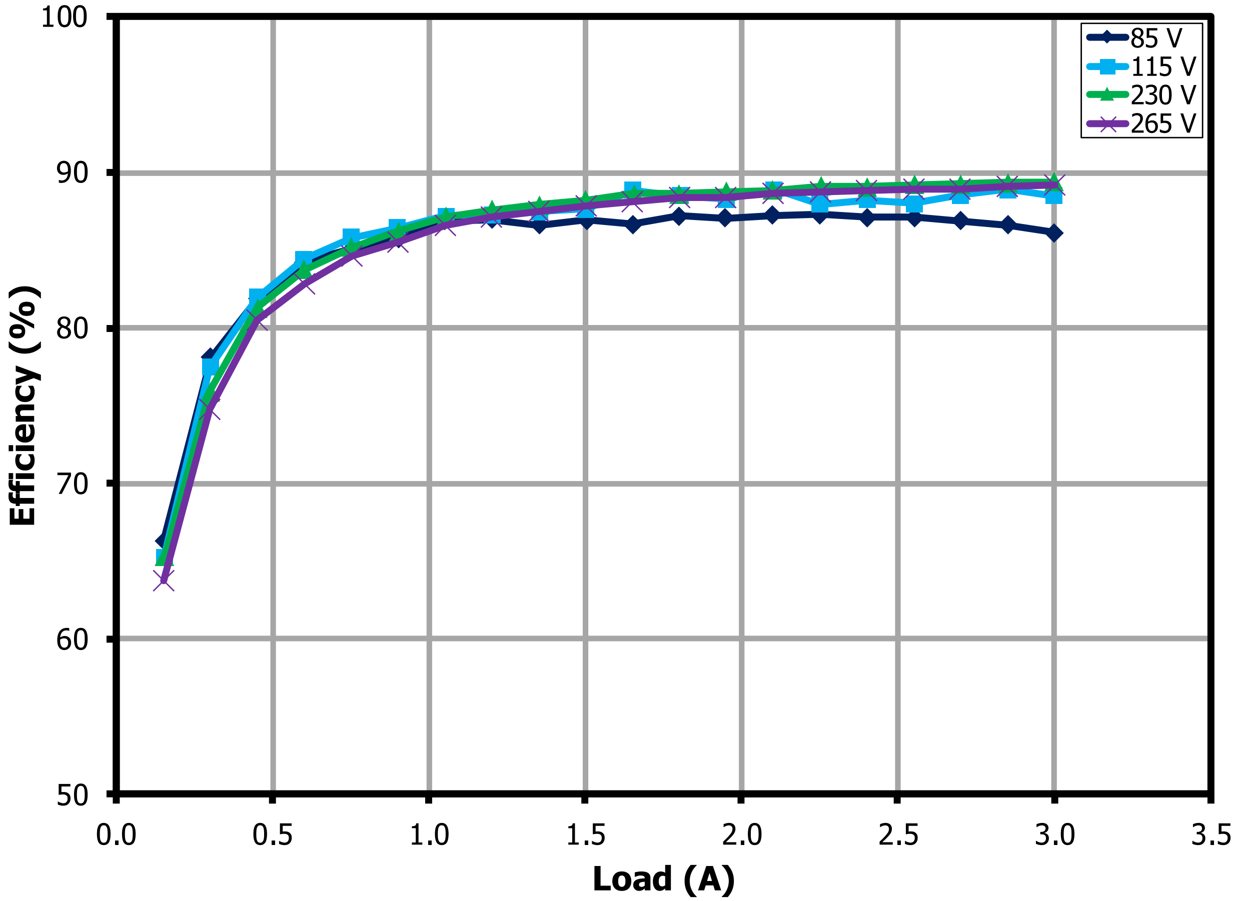

Figure 17 – Efficiency Over Line and Load for 11 V Output.

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10.5.4 *3.0 V Output*

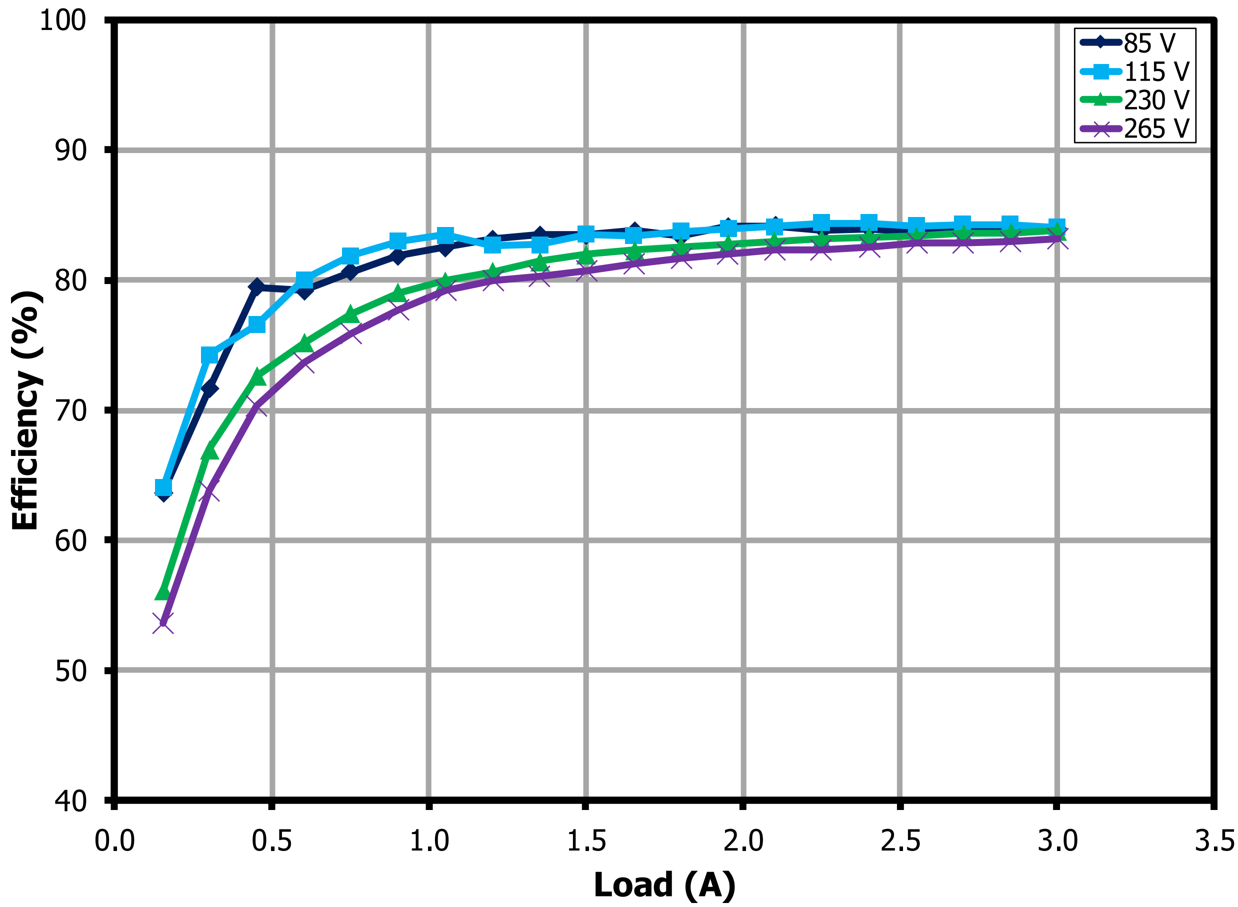

Figure 18 – Efficiency Over Line and Load for 3 V Output.

10.6 Line Regulation (On the Board)

10.6.1 *5.0 V Output*

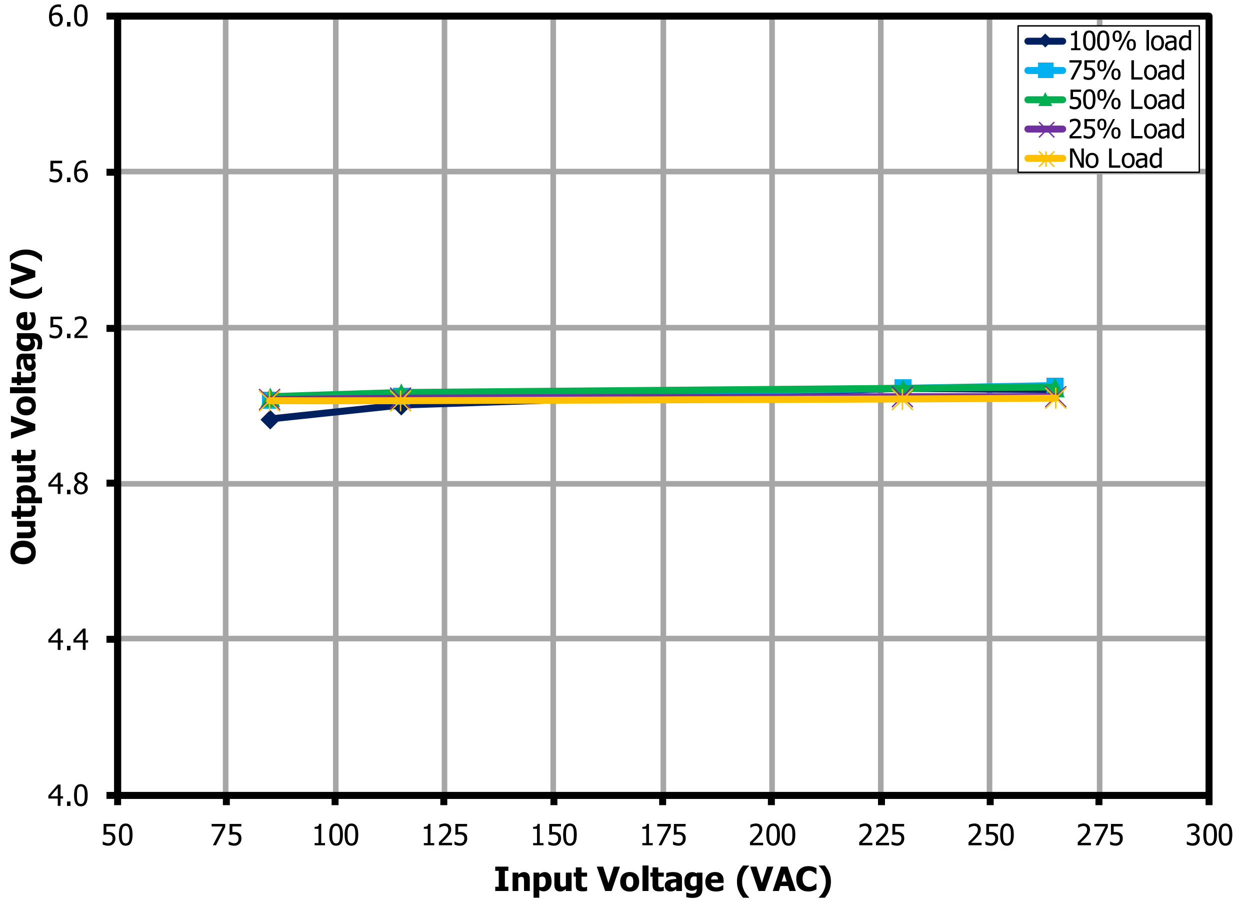

Figure 19 – Output Voltage vs. Input Line Voltage for 5 V Output, Room Temperature.

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10.6.2 *9.0 V Output*

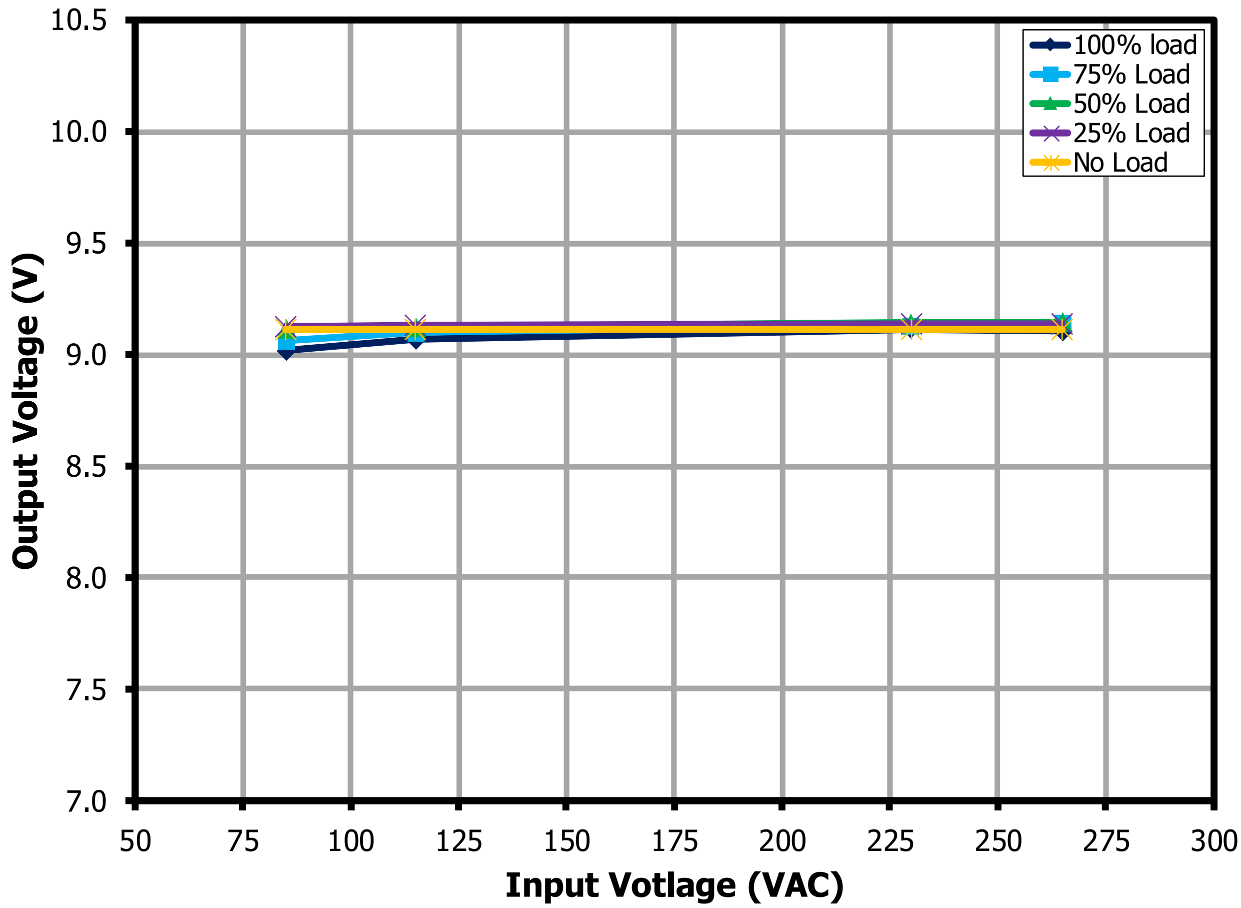

Figure 20 – Output Voltage vs. Input Line Voltage for 9 V Output, Room Temperature.

10.6.3 *11.0 V Output*

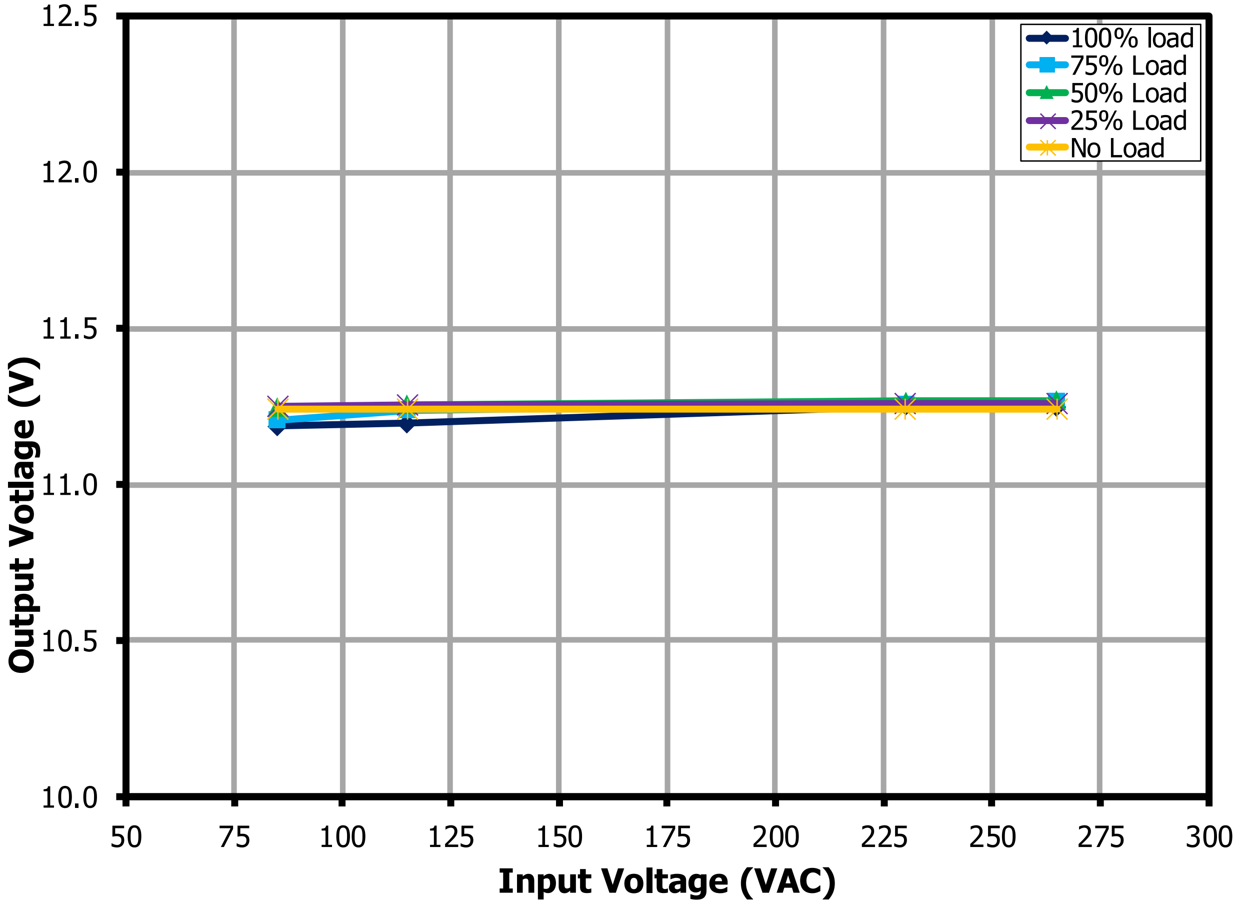

Figure 21 – Output Voltage vs. Input Line Voltage for 9 V Output, Room Temperature.

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10.6.4 *3.0 V Output*

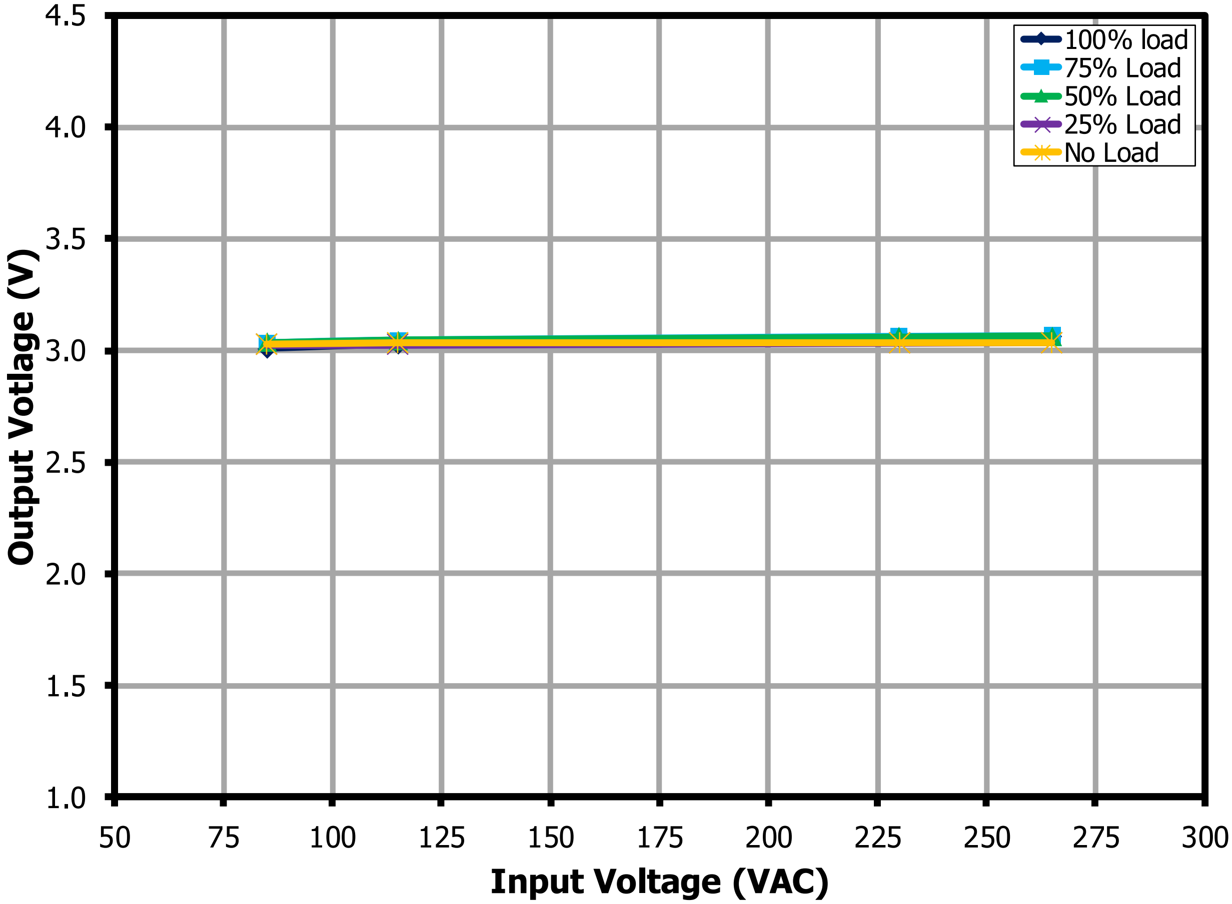

Figure 22 – Output Voltage vs. Input Line Voltage for 9 V Output, Room Temperature.

10.7 **Load Regulation (On the Board)**

10.7.1 *5.0 V Output*

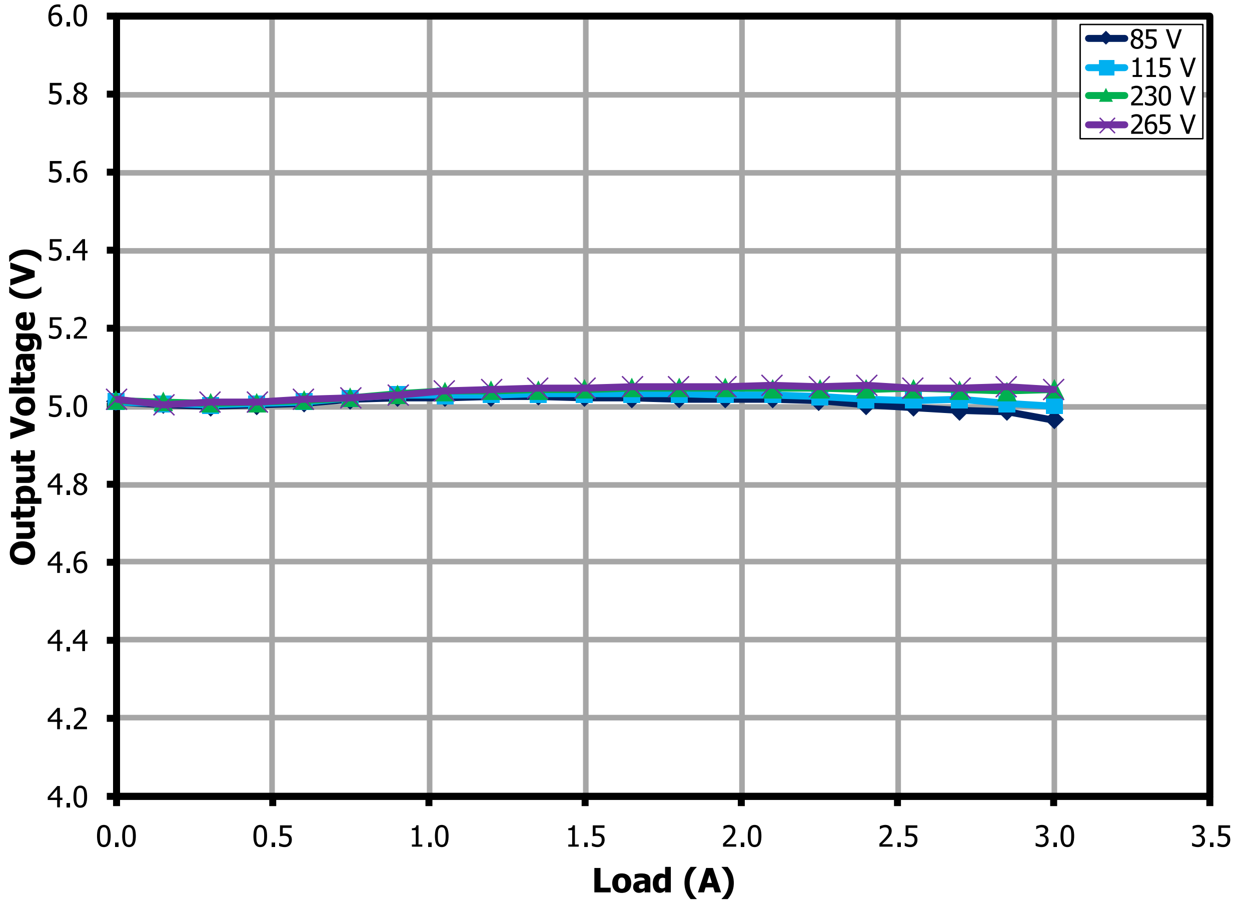

Figure 23 – Output Voltage vs. Output Load for 5 V Output, Room Temperature

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10.7.2 *9.0 V Output*

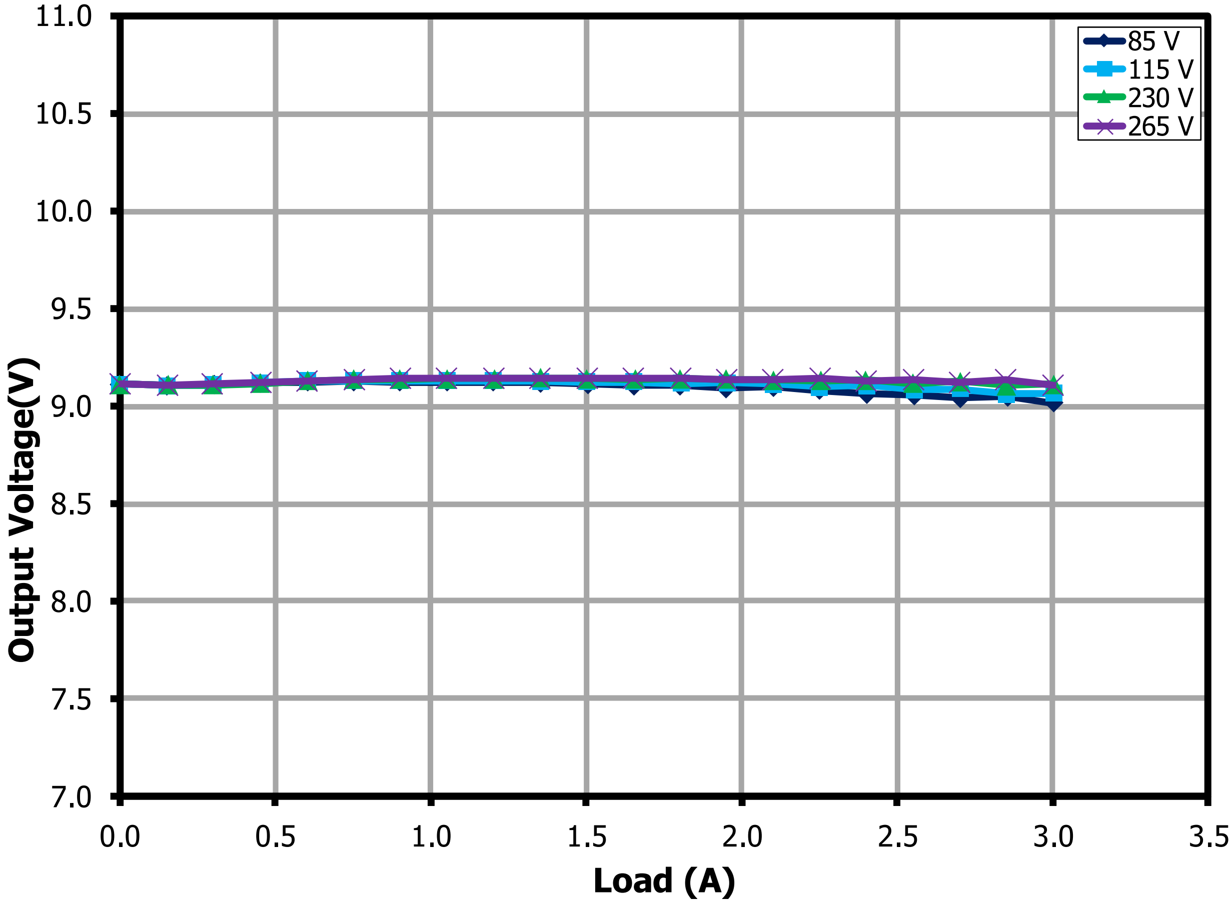

Figure 24 – Output Voltage vs. Output Load for 9 V Output, Room Temperature.

10.7.3 *11.0 V Output*

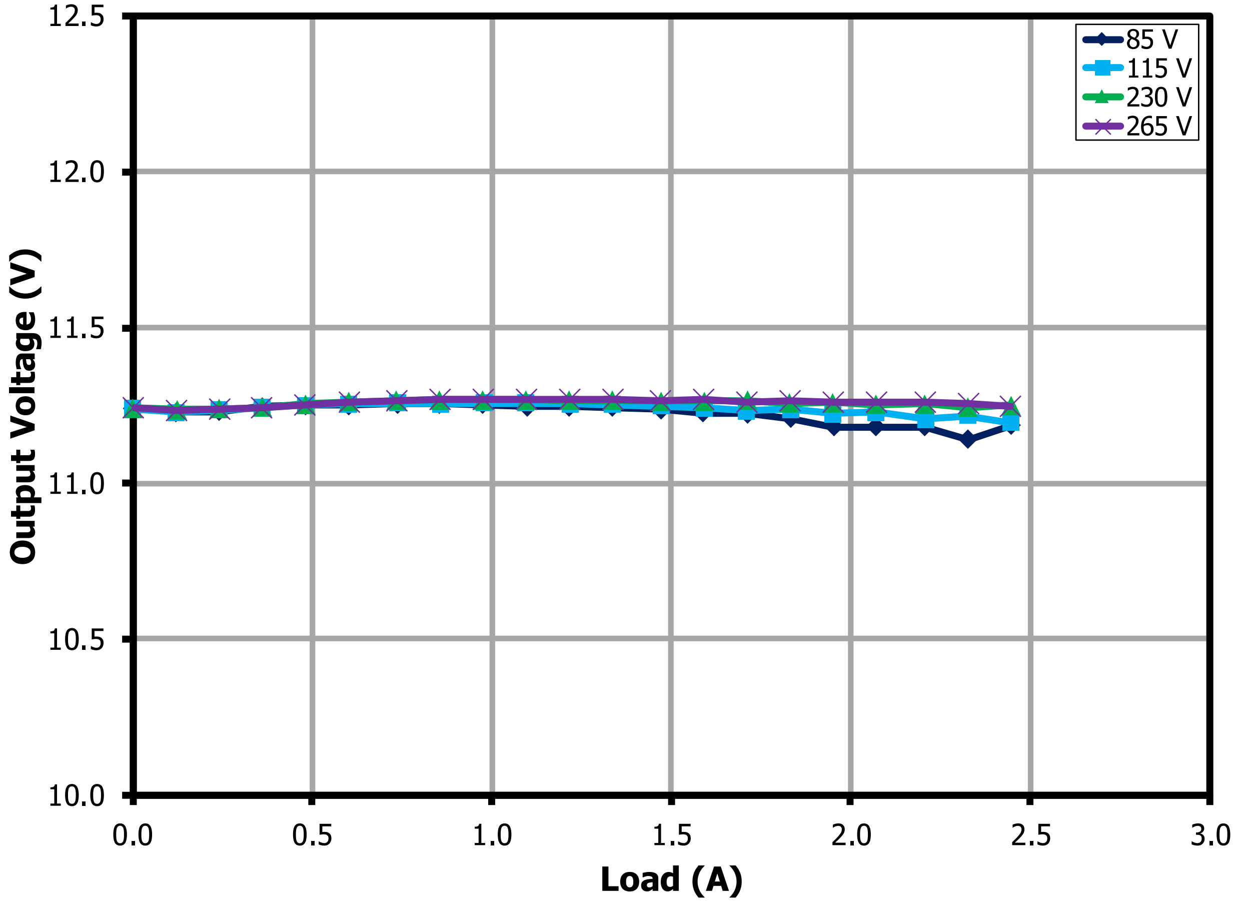

Figure 25 – Output Voltage vs. Output Load for 11 V Output, Room Temperature.

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10.7.4 *3.0 V Output*

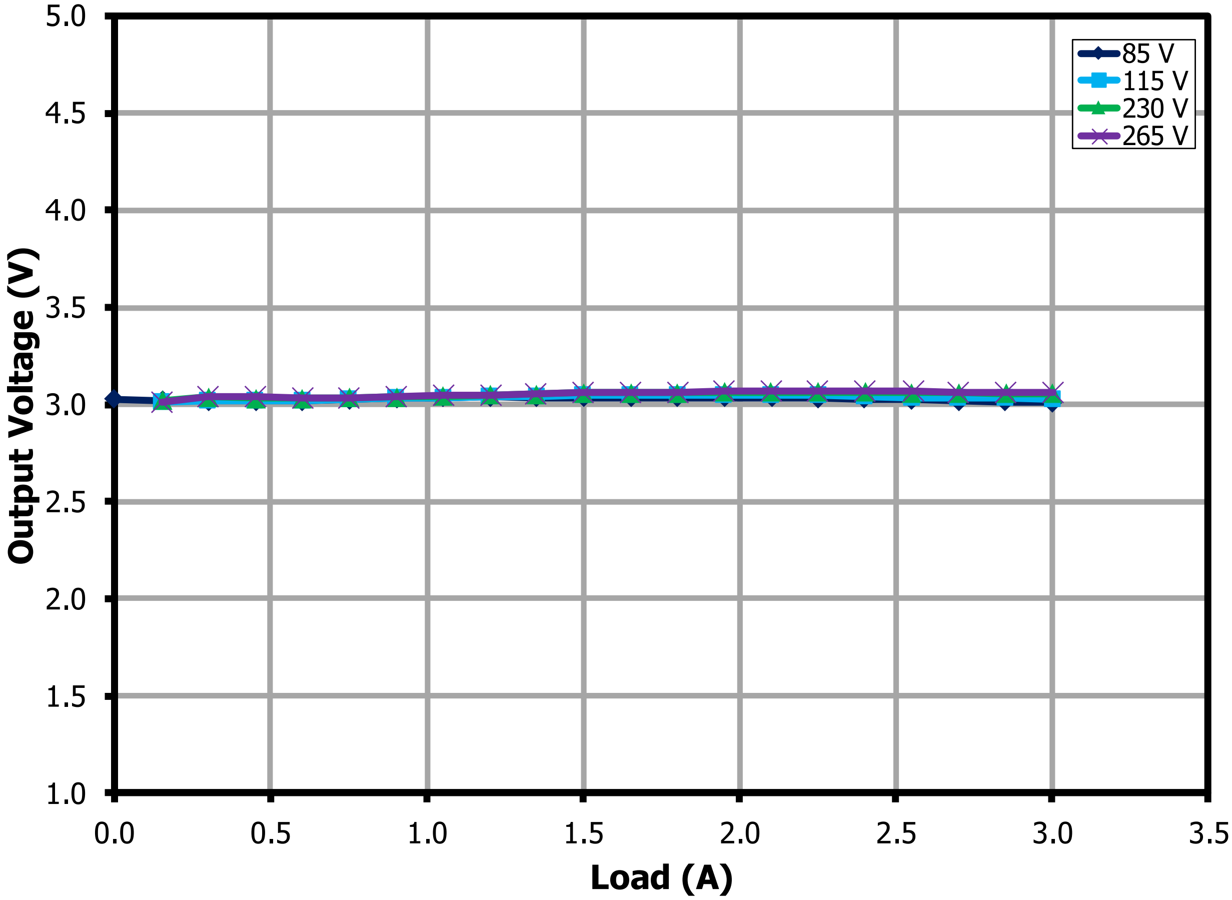

Figure 26 – Output Voltage vs. Output Load for 3 V Output, Room Temperature.

11 CV/CC Plots (On the Board)

11.1.1 *5.0 V Output*

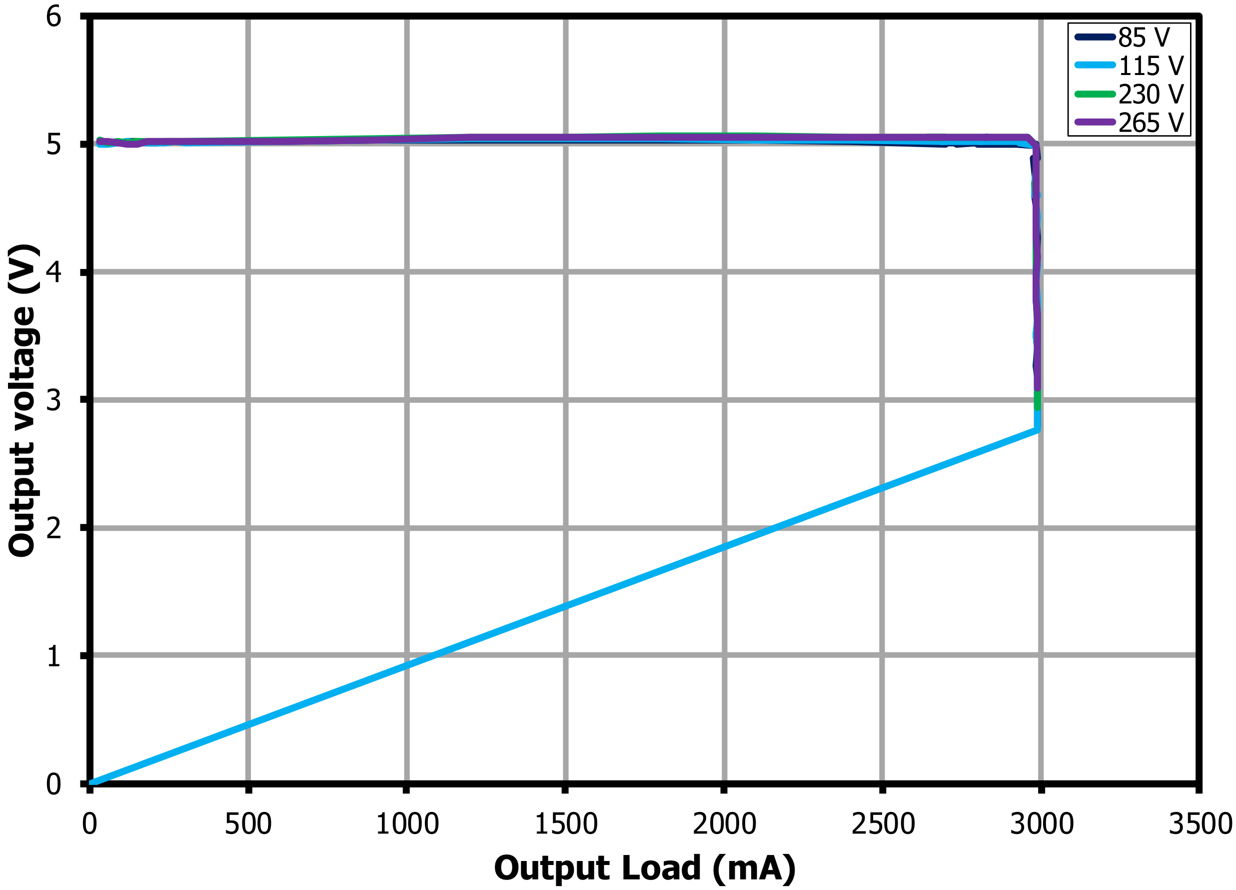

Figure 27 – CV/CC Plot for 5 V Output, Room Temperature.

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11.1.2 *9.0 V Output*

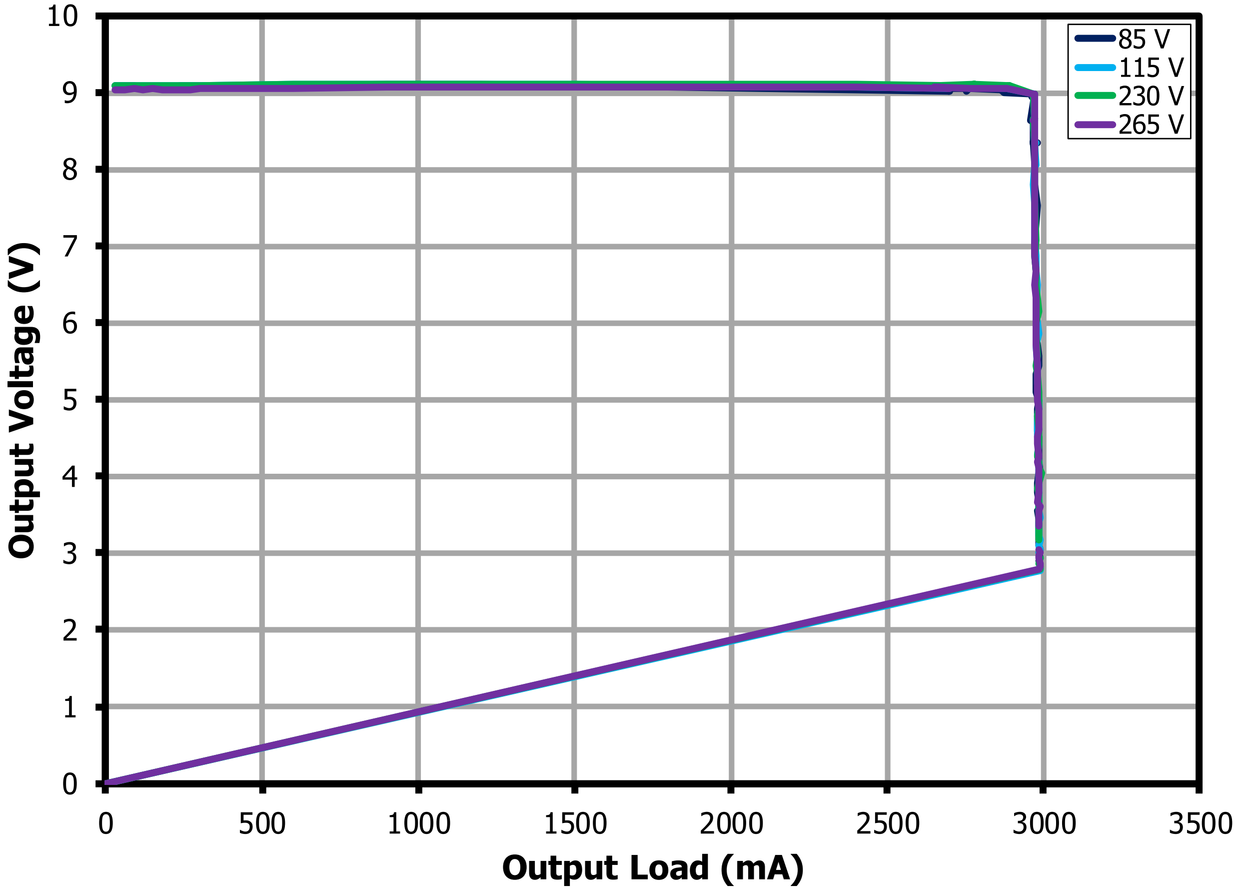

Figure 28 – CV/CC Plot for 9 V Output, Room Temperature.

11.1.3 *3.0 V Output*

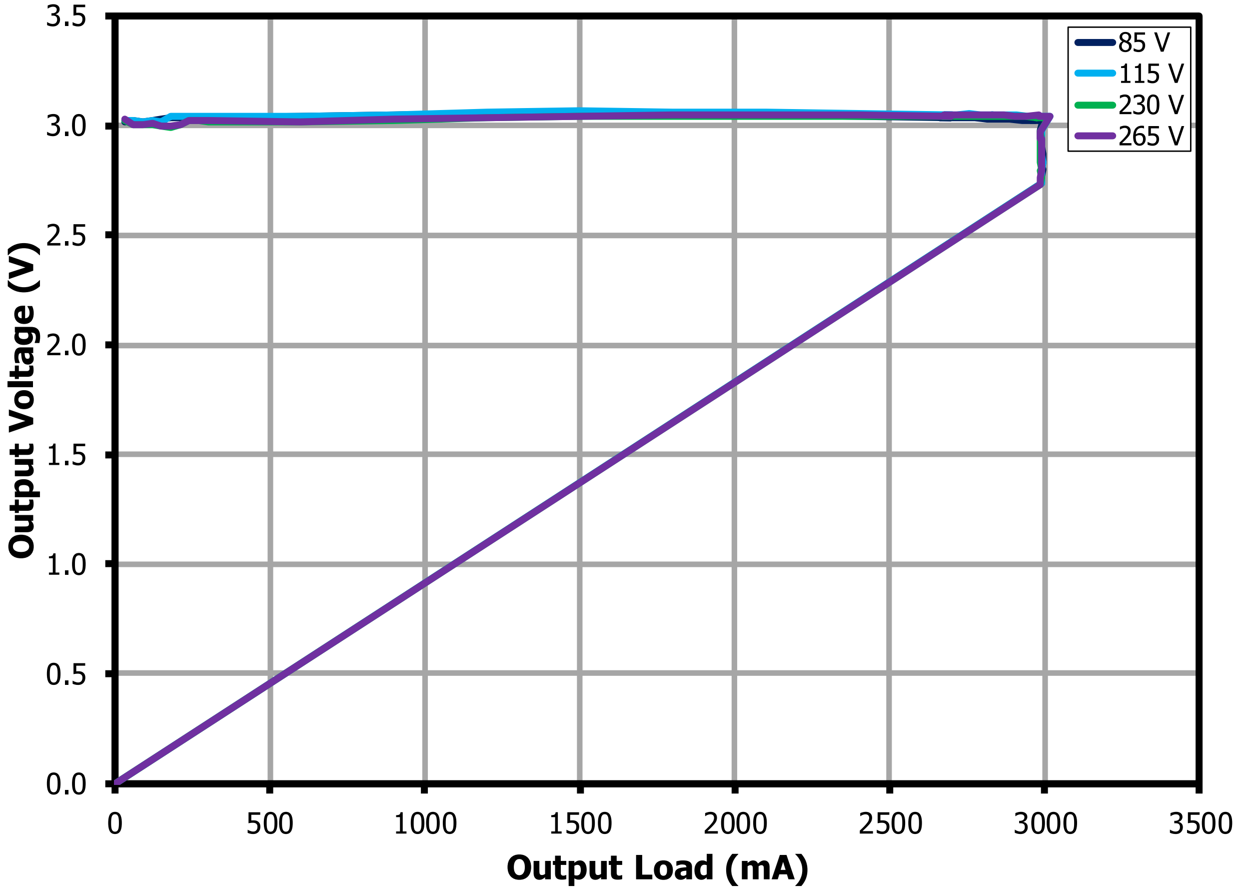

Figure 29 – CV/CC Plot for 3 V Output, Room Temperature.

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11.1.4 *11.0 V Output*

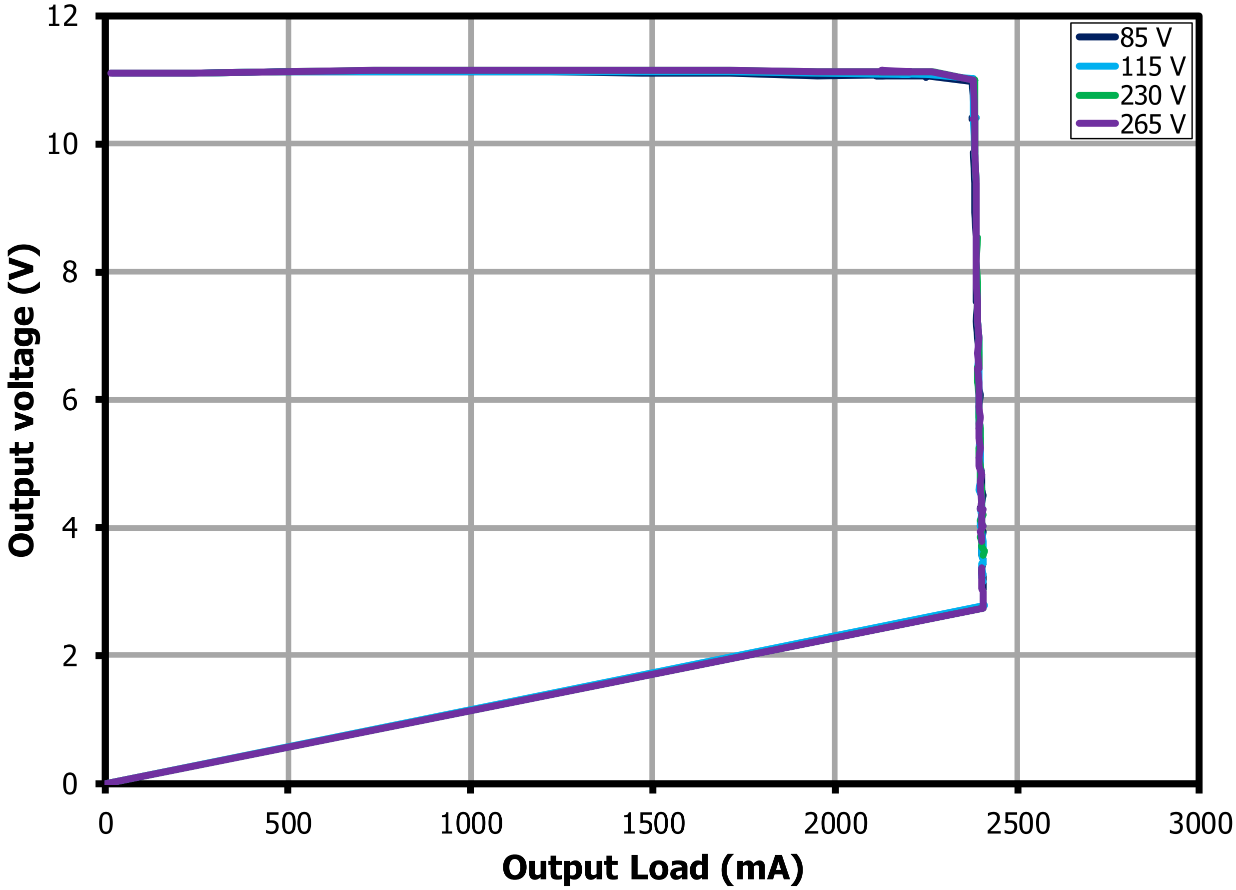

Figure 30 – CV/CC Plot for 11 V Output, Room Temperature.

12 Waveforms

12.1 Load Transient Response (End of Cable)

Figure 31 – Transient Response.
85 VAC, 5.0 V, 0 - 3 A Load Step.
V_{MIN}: 4.614 V, V_{MAX}: 5.059 V.
Upper: V_{OUT}, 0.2 V / div., 200 ms / div.
Lower: I_{LOAD}, 2 A / div.
Zoom: 20 ms / div.

Figure 32 – Transient Response.
115 VAC, 5.0 V, 0 - 3 A Load Step.
V_{MIN}: 4.627 V, V_{MAX}: 5.079 V.
Upper: V_{OUT}, 0.2 V / div., 200 ms / div.
Lower: I_{LOAD}, 2 A / div.
Zoom: 20 ms / div.

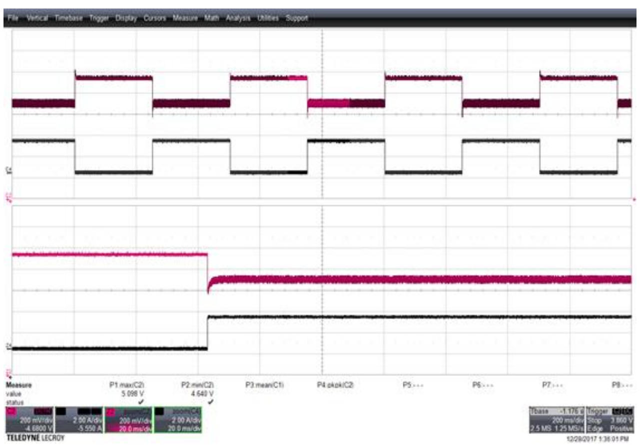

Figure 33 – Transient Response.
230 VAC, 5.0 V, 0 - 3 A Load Step.
V_{MIN}: 4.640 V, V_{MAX}: 5.098 V.
Upper: V_{OUT}, 0.2 V / div., 200 ms / div.
Lower: I_{LOAD}, 2 A / div.
Zoom: 20 ms / div.

Figure 34 – Transient Response.
265 VAC, 5.0 V, 0 - 3 A Load Step.
V_{MIN}: 4.641 V, V_{MAX}: 5.093 V.
Upper: V_{OUT}, 0.2 V / div., 200 ms / div.
Lower: I_{LOAD}, 2 A / div.
Zoom: 20 ms / div.

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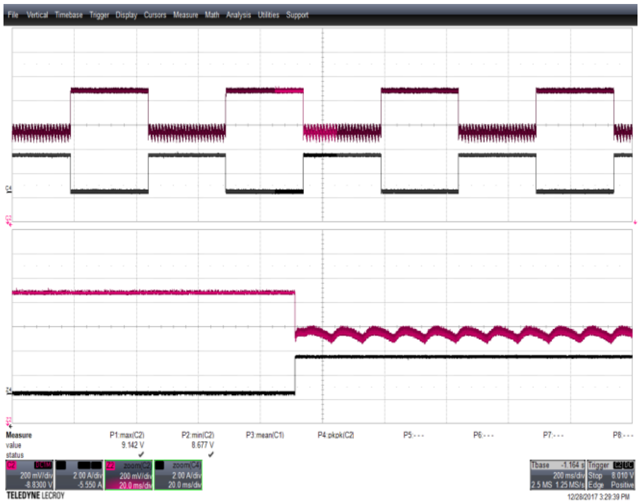

Figure 35 – Transient Response.
85 VAC, 9.0 V, 0 - 3 A Load Step.
V_{MIN}: 8.677 V, V_{MAX}: 9.142 V.
Upper: V_{OUT}, 0.2 V / div., 200 ms / div.
Lower: I_{LOAD}, 2 A / div.
Zoom: 20 ms / div.

Figure 36 – Transient Response.
115 VAC, 9.0 V, 0 - 3 A Load Step.
V_{MIN} 8.644 V, V_{MAX}: 9.149 V.
Upper: V_{OUT}, 0.2 V / div., 200 ms / div.
Lower: I_{LOAD}, 2 A / div.
Zoom: 20 ms / div.

Figure 37 – Transient Response.
230 VAC, 9.0 V, 0 - 3 A Load Step.
V_{MIN}: 8.677 V, V_{MAX}: 9.169 V.
Upper: V_{OUT}, 0.2 V / div., 200 ms / div.
Lower: I_{LOAD}, 2 A / div.
Zoom: 20 ms /div.

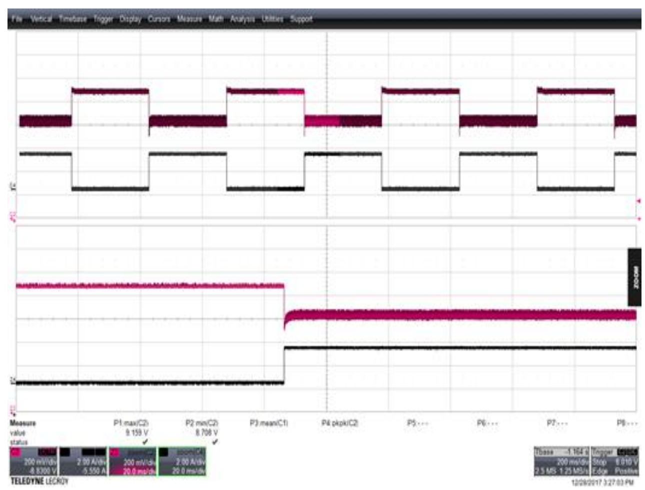

Figure 38 – Transient Response.
265 VAC, 9.0 V, 0 - 3 A Load Step.
V_{MIN}: 9.159V, V_{MAX}: 8.708 V.
Upper: V_{OUT}, 0.2 V / div., 200 ms / div.
Lower: I_{LOAD}, 2 A / div.
Zoom: 20 ms / div.

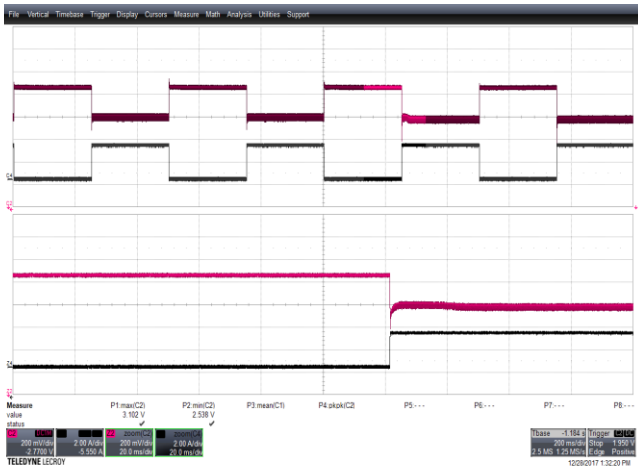

Figure 39 – Transient Response.
85 VAC, 3.0 V, 0 - 3 A Load Step.
V_{MIN}: 2.538 V, V_{MAX}: 3.102 V.
Upper: V_{OUT}, 0.2 V / div., 200 ms / div.
Lower: I_{LOAD}, 2 A / div.
Zoom: 20 ms / div.

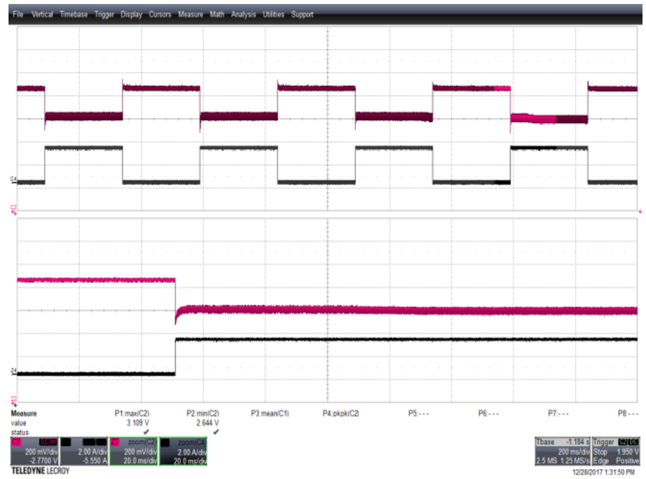

Figure 40 – Transient Response.
115 VAC, 3.0 V, 0 - 3 A Load Step.
V_{MIN}: 2.644 V, V_{MAX}: 3.109 V.
Upper: V_{OUT}, 0.2 V / div., 200 ms / div.
Lower: I_{LOAD}, 2 A / div.
Zoom: 20ms / div.

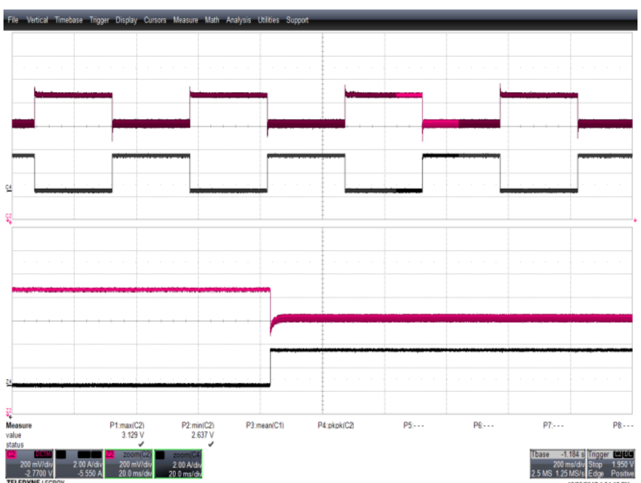

Figure 41 – Transient Response.
230 VAC, 3.0 V, 0 - 3 A Load Step.
V_{MIN}: 3.129 V, V_{MAX}: 2.637 V.
Upper: V_{OUT}, 0.2 V / div., 200 ms / div.
Lower: I_{LOAD}, 2 A / div.
Zoom: 20ms / div.

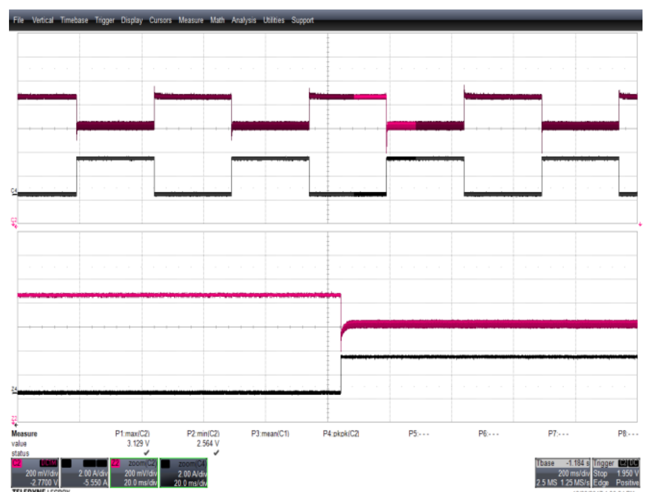

Figure 42 – Transient Response.
265 VAC, 3.0 V, 0 - 3 A Load Step.
V_{MIN}: 3.129, V_{MAX}: 2.564 V.
Upper: V_{OUT}, 0.2 V / div., 200 ms / div.
Lower: I_{LOAD}, 2 A / div.
Zoom: 20 ms / div.

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Figure 43 – Transient Response.
85 VAC, 11.0 V, 0 – 2.45 A Load Step.
V_{MIN}: 10.754 V, V_{MAX}: 11.179 V.
Upper: V_{OUT}, 0.2 V / div., 200 ms / div.
Lower: I_{LOAD}, 2 A / div.
Zoom: 20 ms / div.

Figure 44 – Transient Response.
115 VAC, 11.0 V, 0 – 2.45 A Load Step.
V_{MIN}: 10.798 V, V_{MAX}: 11.190 V.
Upper: V_{OUT}, 0.2 V / div., 200 ms / div.
Lower: I_{LOAD}, 2 A / div.
Zoom: 20 ms / div.

Figure 45 – Transient Response.
230 VAC, 11.0 V, 0 – 2.45 A Load Step.
V_{MIN}: 10.805 V, V_{MAX}: 11.203 V.
Upper: V_{OUT}, 0.2 V / div., 200 ms / div.
Lower: I_{LOAD}, 2 A / div.
Zoom: 20 ms / div.

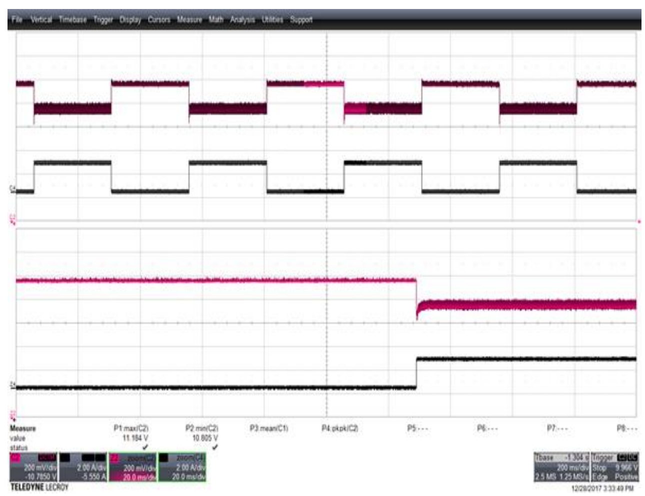

Figure 46 – Transient Response.
265 VAC, 11.0 V, 0 – 2.45 A Load Step.
V_{MIN}: 10.805, V_{MAX}: 11.184 V.
Upper: V_{OUT}, 0.2 V / div., 200 ms / div.
Lower: I_{LOAD}, 2 A / div.
Zoom: 20 ms / div.

12.2 **Switching Waveforms**

12.2.1 *Primary Drain Voltage and Current*

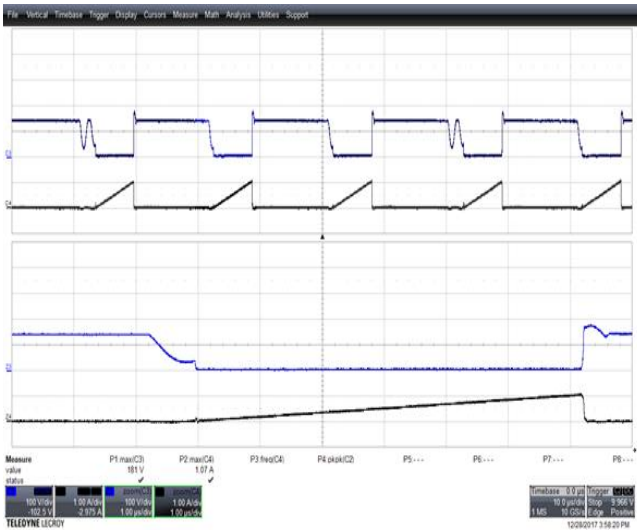

Figure 47 – Drain Voltage and Current Waveforms.
85 VAC, 5.0 V, 3 A Load, (181 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 μs / div.
Lower: I_{DRAIN}, 1 A / div.
Zoom: 1 μs / div.

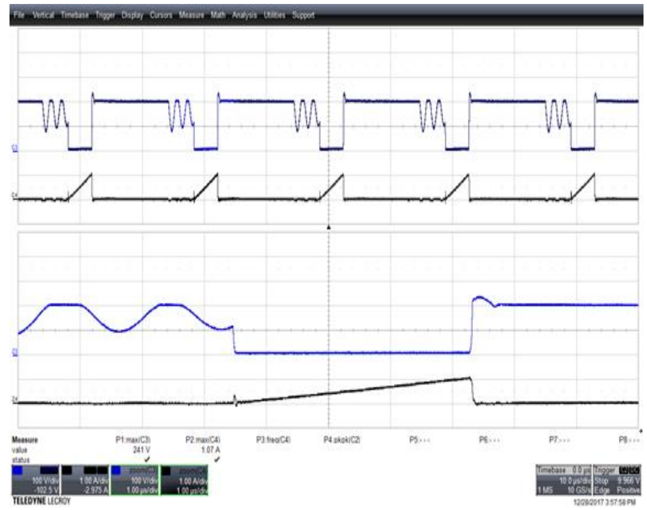

Figure 48 – Drain Voltage and Current Waveforms.
115 VAC, 5.0 V, 3 A Load, (241 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 μs / div.
Lower: I_{DRAIN}, 1 A / div.
Zoom: 1 μs / div.

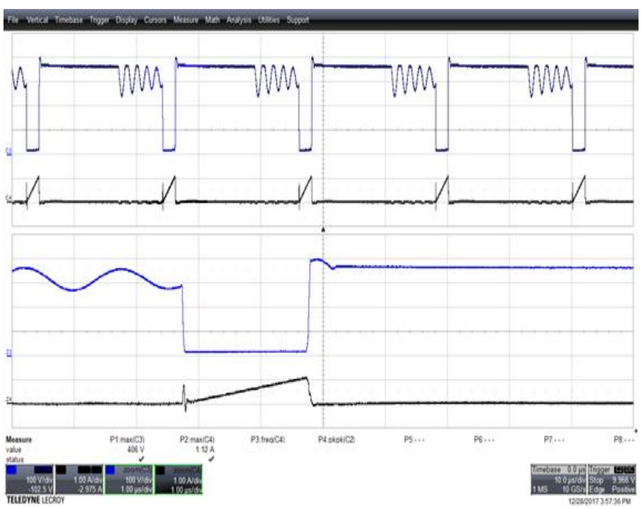

Figure 49 – Drain Voltage and Current Waveforms.
230 VAC, 5.0 V, 3 A Load, (406 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 μs / div.
Lower: I_{DRAIN}, 1 A / div.
Zoom: 1 μs / div.

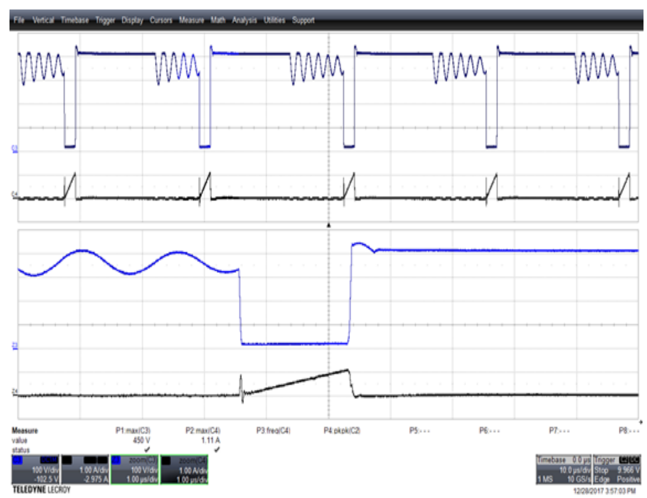

Figure 50 – Drain Voltage and Current Waveforms.
265 VAC, 5.0 V, 3 A Load, (450 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 μs / div.
Lower: I_{DRAIN}, 1 A / div.
Zoom: 1 μs / div.

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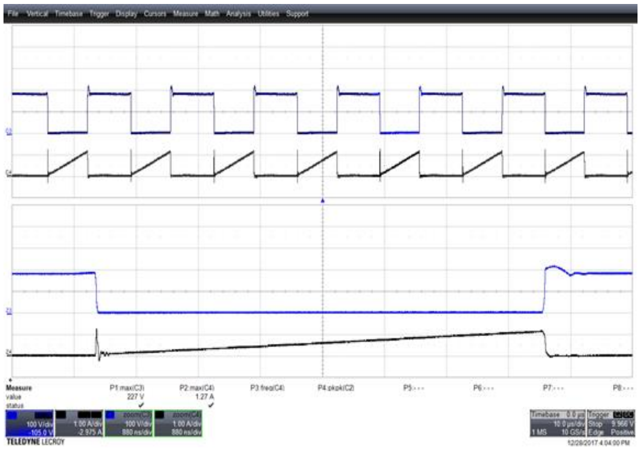

Figure 51 – Drain Voltage and Current Waveforms.
85 VAC, 9.0 V, 3 A Load, (227 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 1 A / div.
Zoom: 880 ns / div.

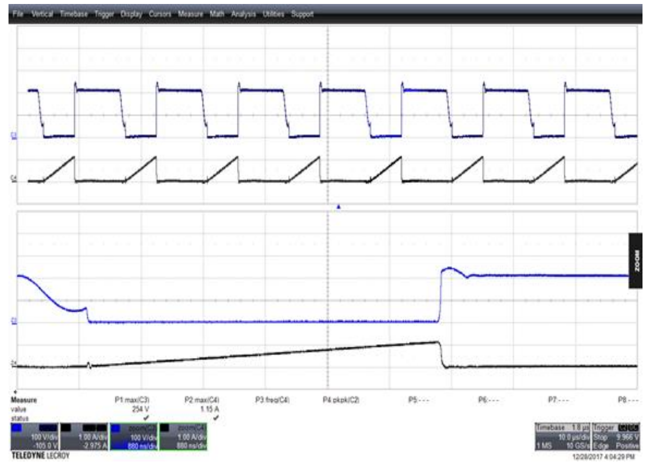

Figure 52 – Drain Voltage and Current Waveforms.
115 VAC, 9.0 V, 3 A Load, (254 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 1 A / div.
Zoom: 880 ns / div.

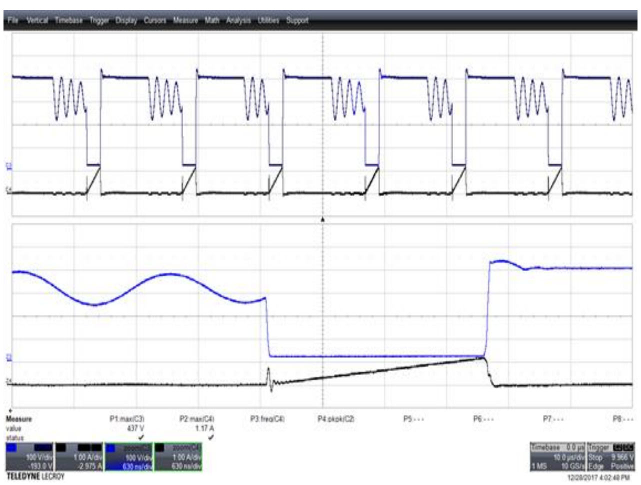

Figure 53 – Drain Voltage and Current Waveforms.
230 VAC, 9.0 V, 3 A Load, (437 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 1 A / div.
Zoom: 630 ns / div.

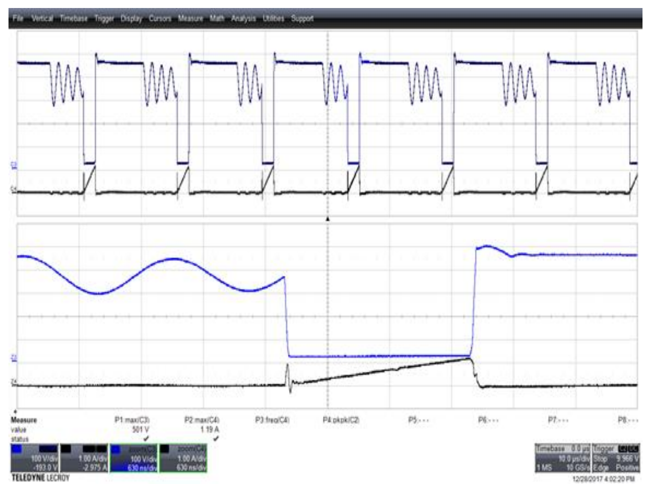

Figure 54 – Drain Voltage and Current Waveforms.
265 VAC, 9.0 V, 3 A Load, (501 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 1 A / div.
Zoom: 630 ns / div.

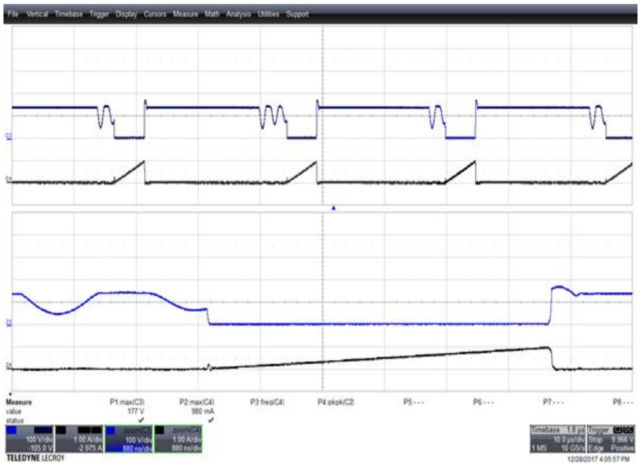

Figure 55 – Drain Voltage and Current Waveforms.
85 VAC, 3.0 V, 3 A Load, (177 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 1 A / div.
Zoom: 880 ns / div.

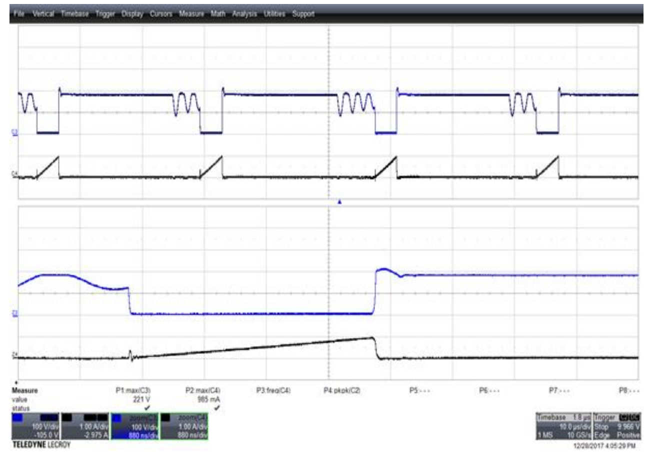

Figure 56 – Drain Voltage and Current Waveforms.
115 VAC, 3.0 V, 3 A Load, (221 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 1 A / div.
Zoom: 880 ns / div.

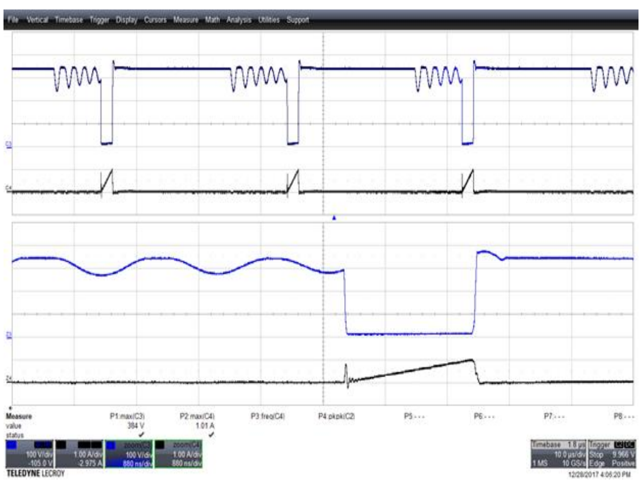

Figure 57 – Drain Voltage and Current Waveforms.
230 VAC, 3.0 V, 3 A Load, (384 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 1 A / div.
Zoom: 880 ns / div.

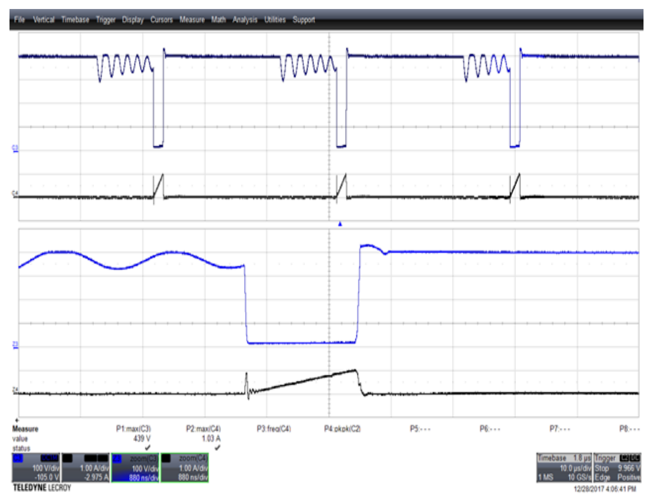

Figure 58 – Drain Voltage and Current Waveforms.
265 VAC, 3.0 V, 3 A Load, (439 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 1 A / div.
Zoom: 880 ns / div.

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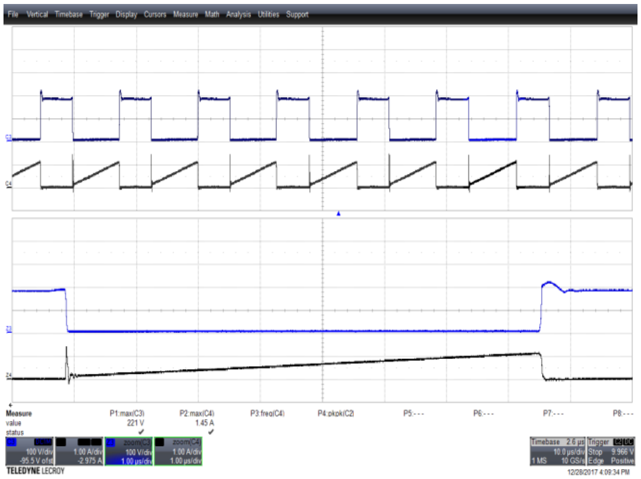

Figure 59 – Drain Voltage and Current Waveforms.
85 VAC, 11.0 V, 2.45 A Load, (221 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 1 A / div.
Zoom: 1 µs / div.

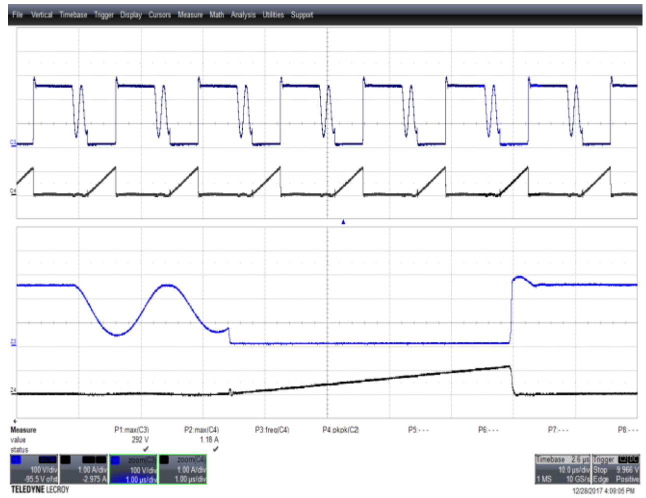

Figure 60 – Drain Voltage and Current Waveforms.
115 VAC, 11.0 V, 2.45 A Load, (292 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 1 A / div.
Zoom: 1 µs / div.

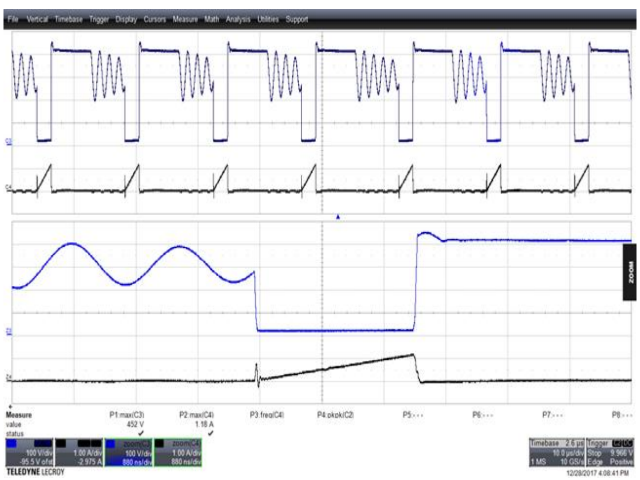

Figure 61 – Drain Voltage and Current Waveforms.
230 VAC, 11.0 V, 2.45 A Load, (452 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 1 A / div.
Zoom: 880 ns / div.

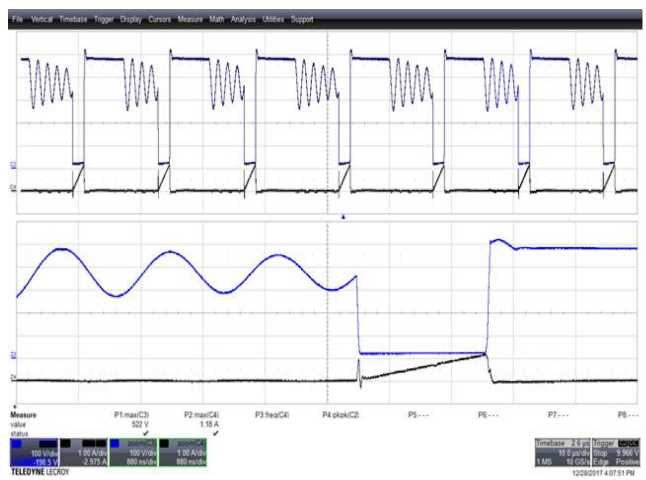

Figure 62 – Drain Voltage and Current Waveforms.
265 VAC, 11.0 V, 2.45 A Load, (522 V_{MAX}).
Upper: V_{DRAIN}, 100 V, 10 µs / div.
Lower: I_{DRAIN}, 1 A / div.
Zoom: 880 ns / div.

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12.2.2 *SR FET Drain Voltage and Current*

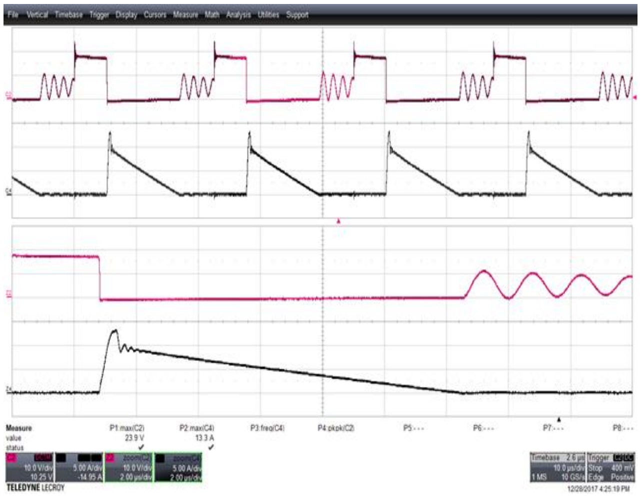

Figure 63 – SR FET Drain Voltage and Current Waveforms.
85 VAC, 5.0 V, 3 A Load, (23.9 V_{MAX}).
Upper: V_{SR_DRAIN}, 10 V, 10 µs / div.
Lower: I_{SR_DRAIN}, 5 A / div.
Zoom: 2 µs / div.

Figure 64 – SR FET Drain Voltage and Current Waveforms.
115 VAC, 5.0 V, 3 A Load, (30.8 V_{MAX}).
Upper: V_{SR_DRAIN}, 10 V, 10 µs / div.
Lower: I_{SR_DRAIN}, 5 A / div.
Zoom: 2 µs / div.

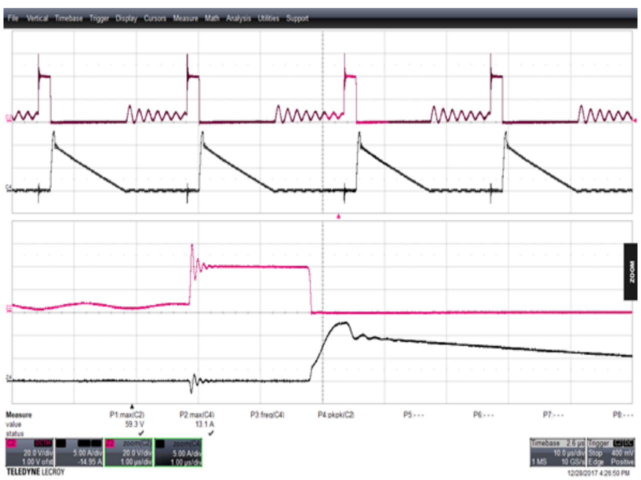

Figure 65 – SR FET Drain Voltage and Current Waveforms.
230 VAC, 5.0 V, 3 A Load, (59.3 V_{MAX}).
Upper: V_{SR_DRAIN}, 20 V, 10 µs / div.
Lower: I_{SR_DRAIN}, 5 A / div.
Zoom: 1 µs / div.

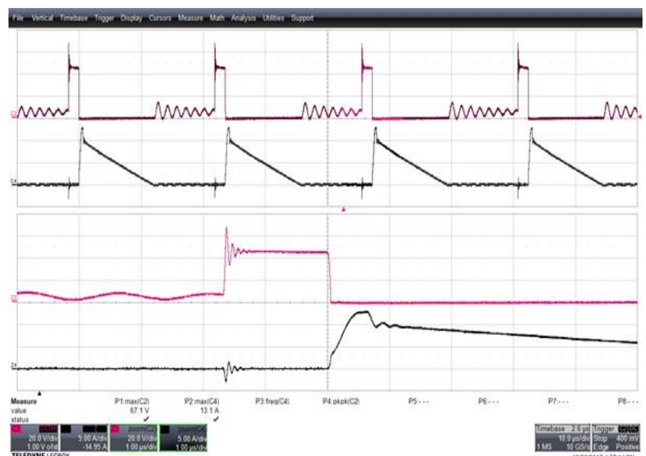

Figure 66 – SR FET Drain Voltage and Current Waveforms.
265 VAC, 5.0 V, 3 A Load, (67.1 V_{MAX}).
Upper: V_{SR_DRAIN}, 20 V, 10 µs / div.
Lower: I_{SR_DRAIN}, 5 A / div.
Zoom: 2 µs / div.

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Figure 67 – SR FET Drain Voltage and Current Waveforms.
85 VAC, 9.0 V, 3 A Load, (32.7 V_{MAX})
Upper: V_{SR_DRAIN}, 20 V, 10 μs / div.
Lower: I_{SR_DRAIN}, 5 A / div.
Zoom: 2 μs / div.

Figure 68 – SR FET Drain Voltage and Current Waveforms.
115 VAC, 9.0 V, 3 A Load, (33.2 V_{MAX}).
Upper: V_{SR_DRAIN}, 20 V, 10 μs / div.
Lower: I_{SR_DRAIN}, 5 A / div.
Zoom: 2 μs / div.

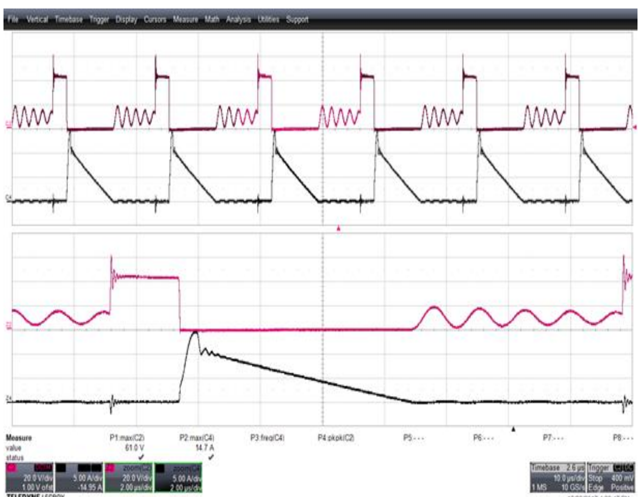

Figure 69 – SR FET Drain Voltage and Current Waveforms.
230 VAC, 9.0 V, 3 A Load, (61 V_{MAX}).
Upper: V_{SR_DRAIN}, 20 V, 10 μs / div.
Lower: I_{SR_DRAIN}, 5 A / div.
Zoom: 2 μs / div.

Figure 70 – SR FET Drain Voltage and Current Waveforms.
265 VAC, 9.0 V, 3 A Load, (70.9 V_{MAX}).
Upper: V_{SR_DRAIN}, 20 V, 10 μs / div.
Lower: I_{SR_DRAIN}, 5 A / div.
Zoom: 2 μs / div.

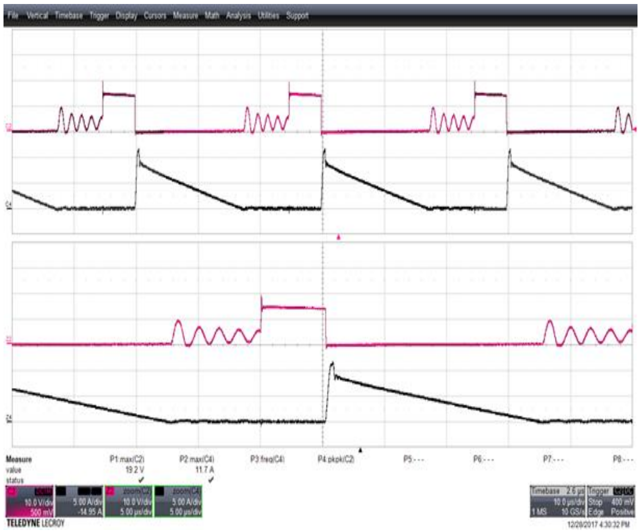

Figure 71 – SR FET Drain Voltage and Current Waveforms.
85 VAC, 3.0 V, 3 A Load, (19.2 V_{MAX}).
Upper: V_{SR_DRAIN}, 10 V,10 μs / div.
Lower: I_{SR_DRAIN}, 5 A / div.
Zoom: 5 μs / div.

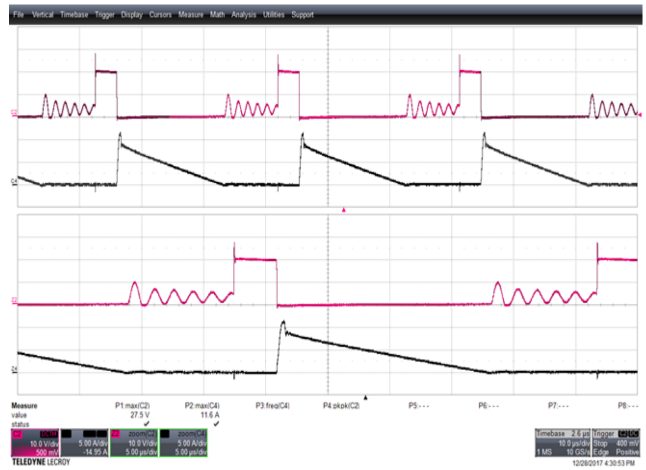

Figure 72 – SR FET Drain Voltage and Current Waveforms.
115 VAC, 3.0 V, 3 A Load, (27.5 V_{MAX}).
Upper: V_{SR_DRAIN}, 10 V, 10 μs / div
Lower: I_{SR_DRAIN}, 5 A / div.
Zoom: 5 μs / div.

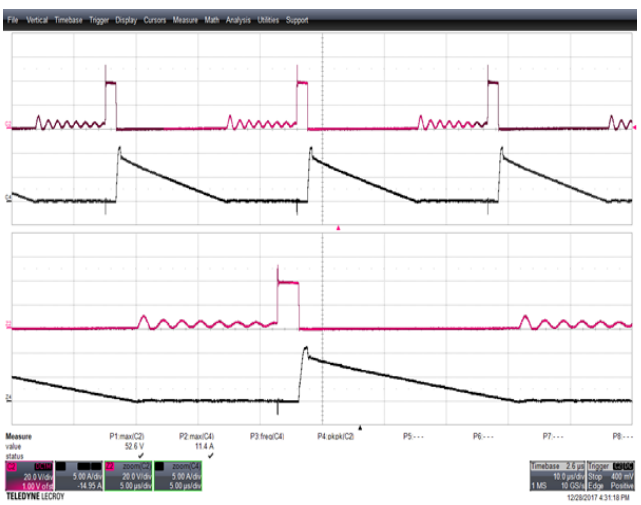

Figure 73 – SR FET Drain Voltage and Current Waveforms.
230 VAC, 3.0 V, 3 A Load, (52.6 V_{MAX}).
Upper: V_{SR_DRAIN}, 20 V, 10 μs / div.
Lower: I_{SR_DRAIN}, 5 A / div.
Zoom: 5 μs / div.

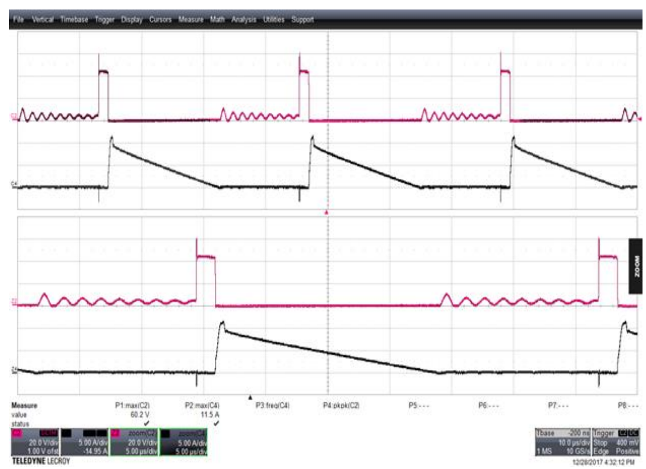

Figure 74 – SR FET Drain Voltage and Current Waveforms.
265 VAC, 3.0 V, 3 A Load, (60.2 V_{MAX}).
Upper: V_{SR_DRAIN}, 20 V, 10 μs / div.
Lower: I_{SR_DRAIN}, 5 A / div.
Zoom: 5 μs / div.

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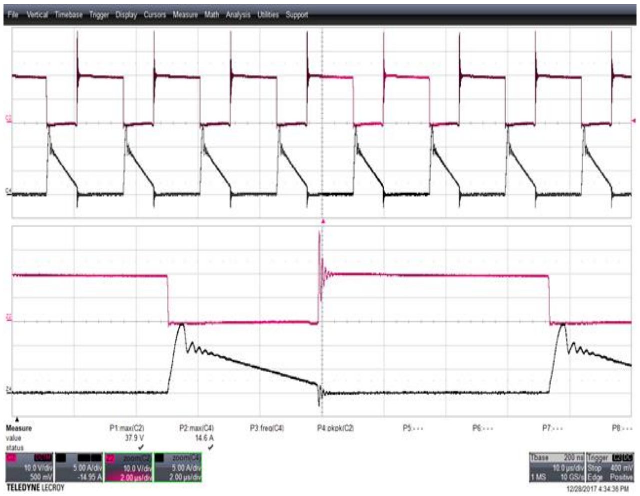

Figure 75 – SR FET Drain Voltage and Current Waveforms.
85 VAC, 11.0 V, 3 A Load, (37.9 V_{MAX}).
Upper: V_{SR_DRAIN}, 10 V, 10 μs / div.
Lower: I_{SR_DRAIN}, 5 A / div.
Zoom: 2 μs / div.

Figure 76 – SR FET Drain Voltage and Current Waveforms.
115 VAC, 11.0 V, 3 A Load, (31.4 V_{MAX}).
Upper: V_{SR_DRAIN}, 10 V, 10 μs / div.
Lower: I_{SR_DRAIN}, 5 A / div.
Zoom: 2 μs / div.

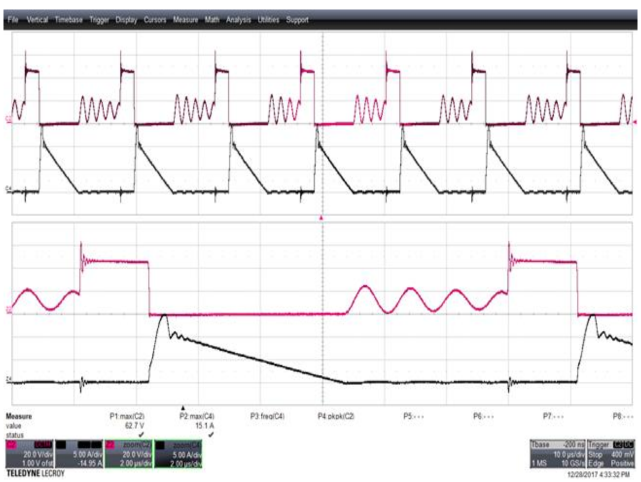

Figure 77 – SR FET Drain Voltage and Current Waveforms.
230 VAC, 11.0 V, 3 A Load, (62.7 V_{MAX}).
Upper: V_{SR_DRAIN}, 20 V, 10 μs / div.
Lower: I_{SR_DRAIN}, 5 A / div.
Zoom: 2 μs / div.

Figure 78 – SR FET Drain Voltage and Current Waveforms.
265 VAC, 11.0 V, 3 A Load, (72.9 V_{MAX}).
Upper: V_{SR_DRAIN}, 20 V, 10 μs / div.
Lower: I_{SR_DRAIN}, 5 A / div.
Zoom: 2 μs / div.

12.3 **Output Ripple Measurements**

12.3.1 *Ripple Measurement Technique*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

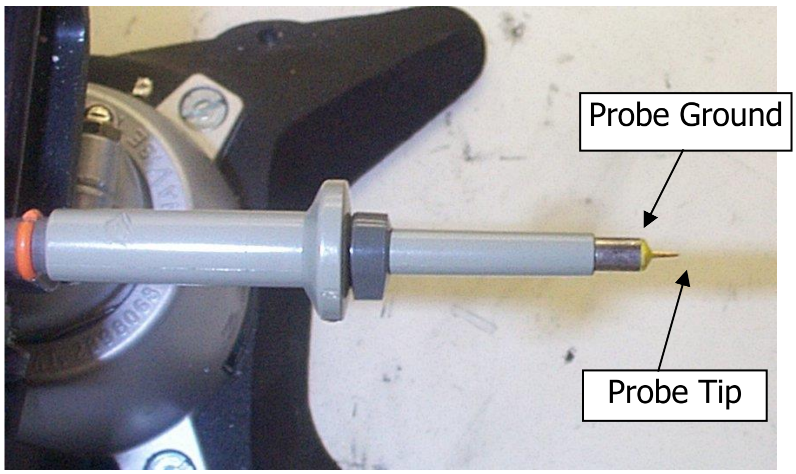

Figure 79 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

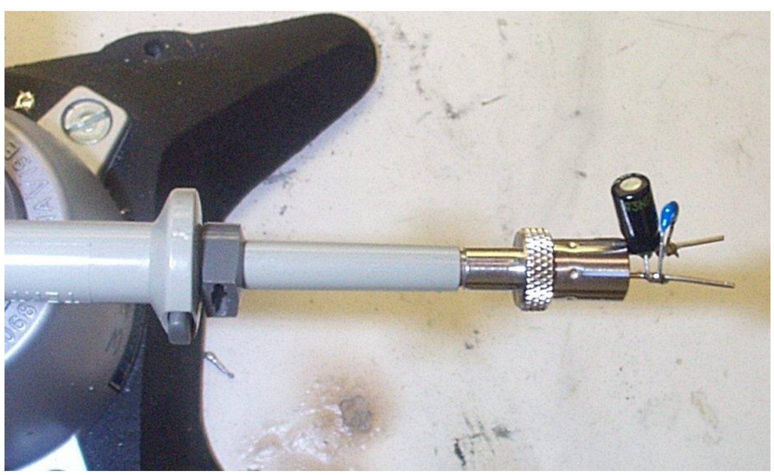

Figure 80 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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12.3.1.1 5 V (End of Type-C Cable)

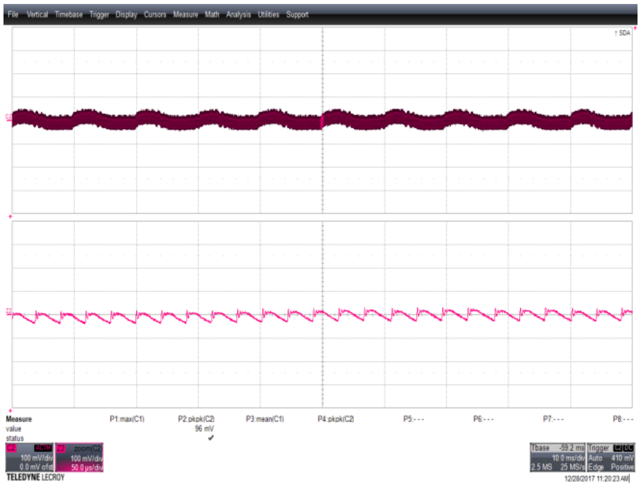

Figure 81 – Output Ripple. PK-PK = 96 mV.
85 VAC Input 5.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.
Zoom: 50 µs / div.

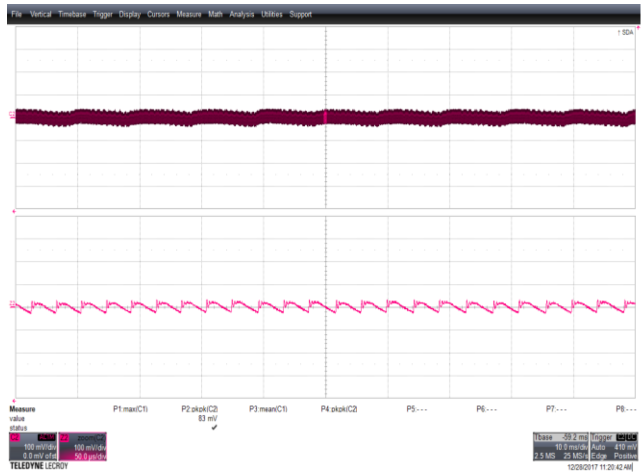

Figure 82 – Output Ripple. PK-PK = 83 mV.
115 VAC Input 5.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.
Zoom: 50 µs / div.

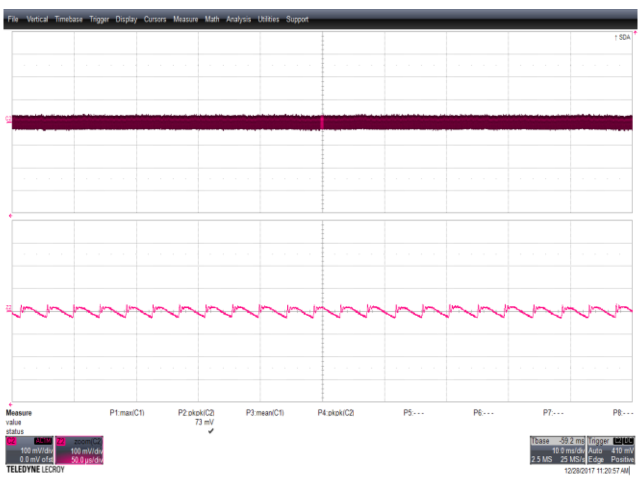

Figure 83 – Output Ripple. PK-PK = 73 mV.
230 VAC Input 5.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.
Zoom: 50 µs / div.

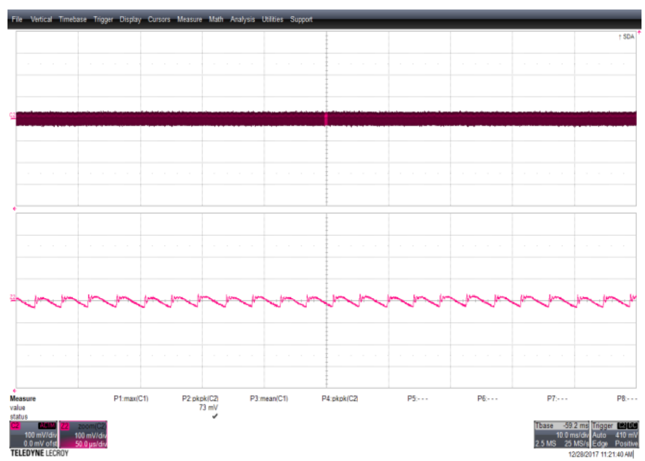

Figure 84 – Output Ripple. PK-PK = 73 mV.
265 VAC Input 5.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.
Zoom: 50 µs / div.

12.3.1.2 9 V (End of Type-C Cable)

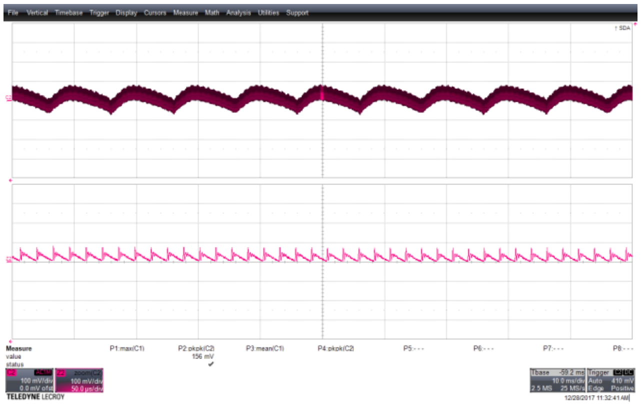

Figure 85 – Output Ripple. PK-PK = 156 mV.
85 VAC Input 9.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.
Zoom: 50 μs / div.

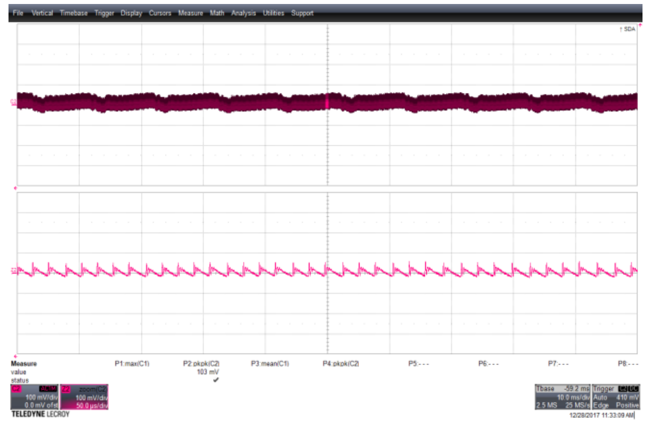

Figure 86 – Output Ripple. PK-PK = 103 mV.
115 VAC Input 9.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.
Zoom: 50 μs / div.

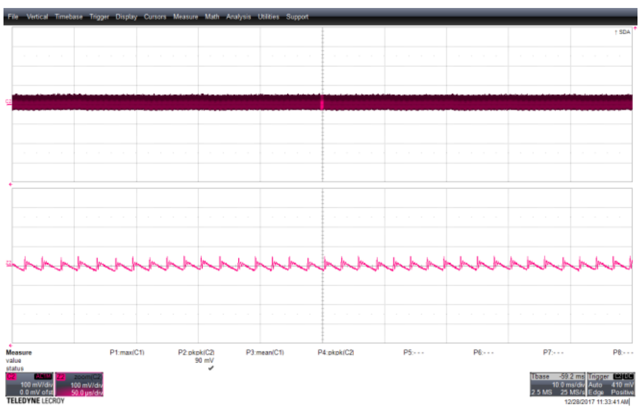

Figure 87 – Output Ripple. PK-PK = 90 mV.
230 VAC Input 9.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.
Zoom: 50 μs / div.

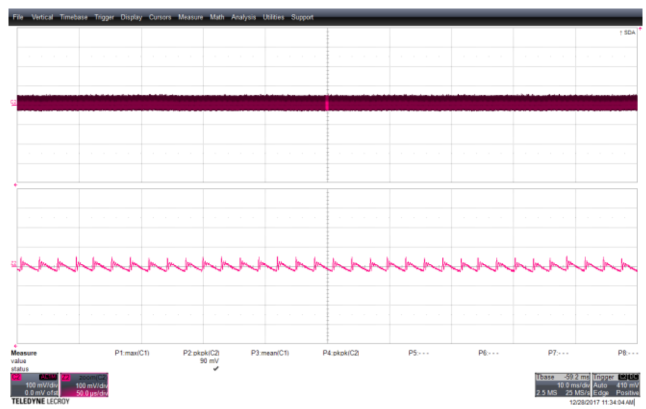

Figure 88 – Output Ripple. PK-PK = 90 mV.
265 VAC Input 9.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.
Zoom: 50 μs / div.

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12.3.1.3 3 V (End of Type-C Cable)

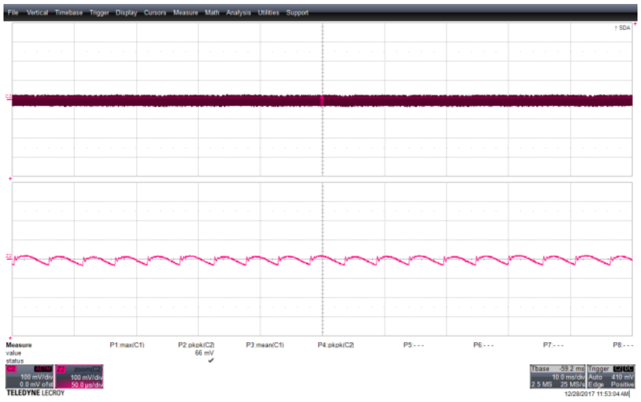

Figure 89 – Output Ripple. PK-PK = 66 mV.
85 VAC Input 3.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.
Zoom: 50 µs / div.

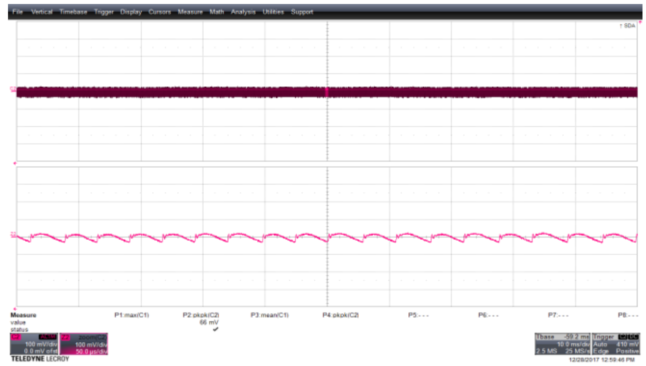

Figure 90 – Output Ripple. PK-PK = 66 mV.
115 VAC Input 3.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.
Zoom: 50 µs / div.

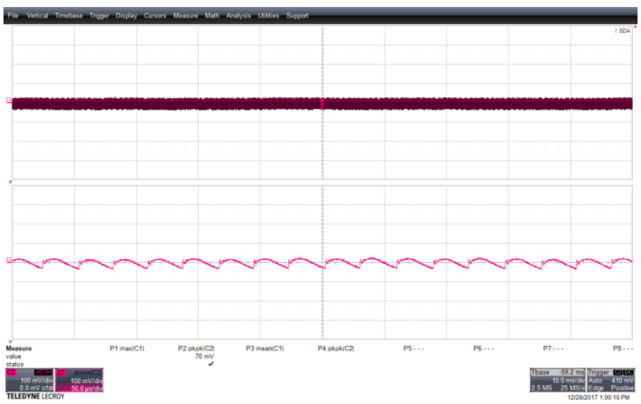

Figure 91 – Output Ripple. PK-PK = 70 mV.
230 VAC Input 3.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.
Zoom: 50 µs / div.

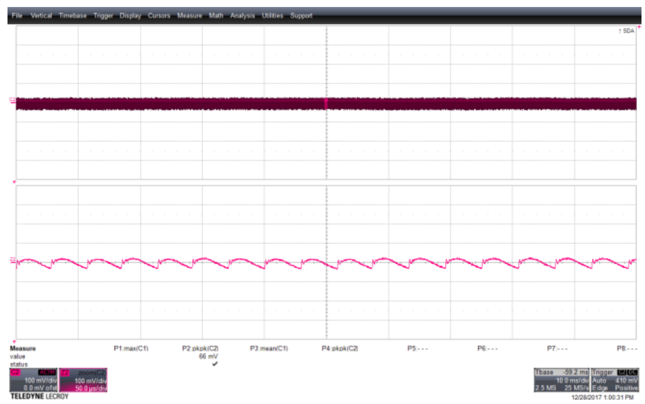

Figure 92 – Output Ripple. PK-PK = 66 mV.
265 VAC Input 3.0 V, 3 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.
Zoom: 50 µs / div.

12.3.1.4 11 V (End of Type-C Cable)

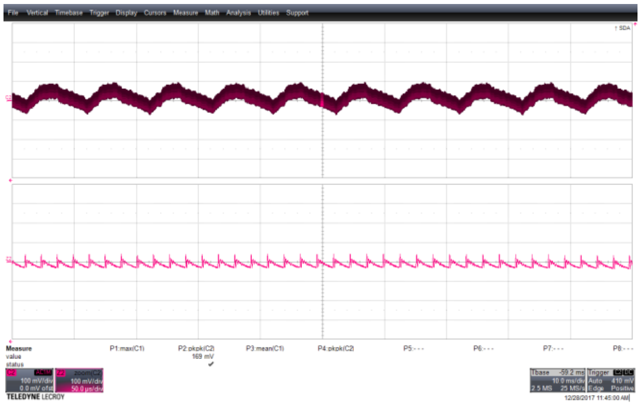

Figure 93 – Output Ripple. PK-PK = 173 mV.
85 VAC Input 11.0 V, 2.45 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.
Zoom: 50 μs / div.

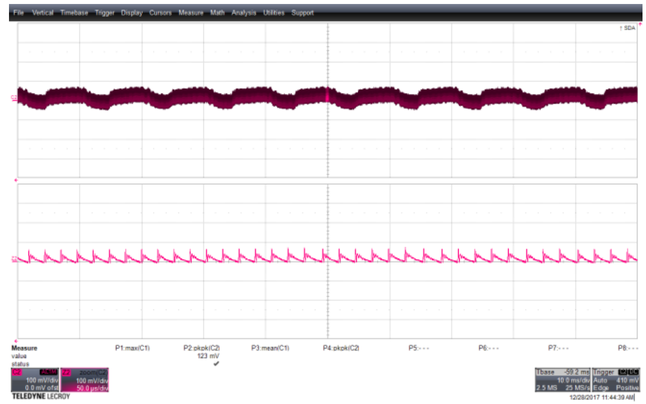

Figure 94 – Output Ripple. PK-PK = 123 mV.
115 VAC Input 11.0 V, 2.45 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.
Zoom: 50 μs / div.

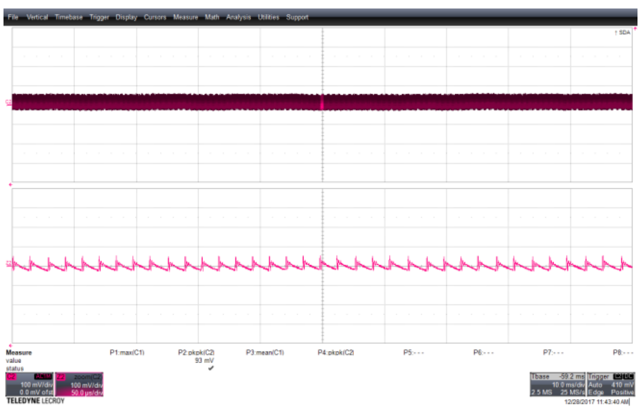

Figure 95 – Output Ripple. PK-PK = 93 mV.
230 VAC Input 11.0 V, 2.45 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.
Zoom: 50 μs / div.

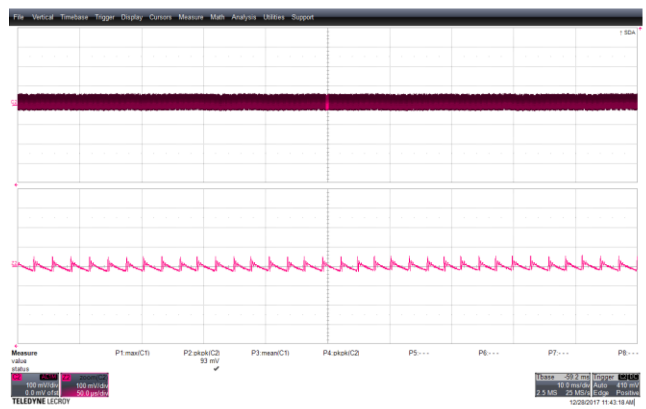

Figure 96 – Output Ripple. PK-PK = 93 mV.
265 VAC Input 11.0 V, 2.45 A Load.
V_{OUT}, 100 mV / div., 10 ms / div.
Zoom: 50 μs / div.

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12.3.1.5 Output Voltage Ripple Plots for 5 V (End of Type-C Cable)

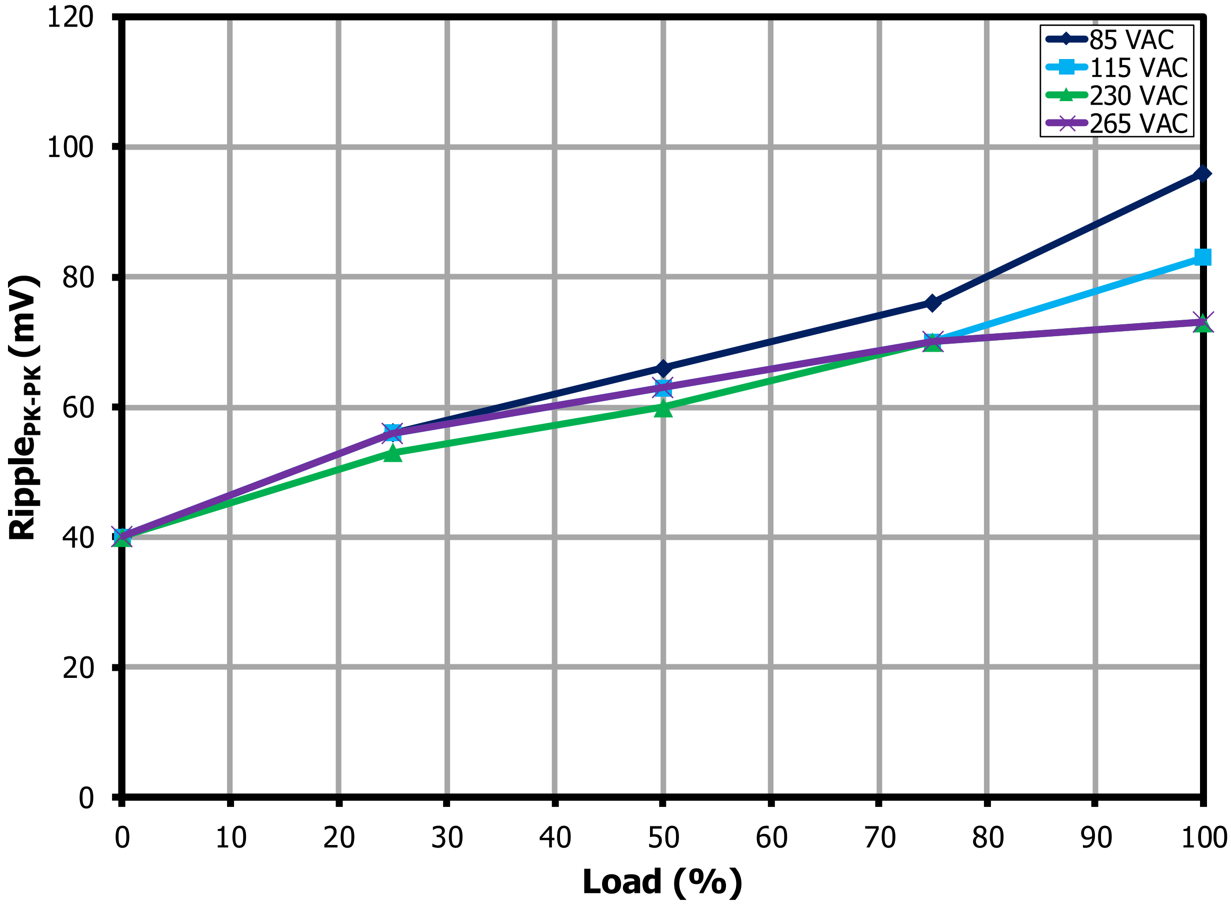

Figure 97 – Output Voltage Ripple Plots for 5 V.

12.3.1.6 Output Voltage Ripple Plots for 9 V (End of Type-C Cable)

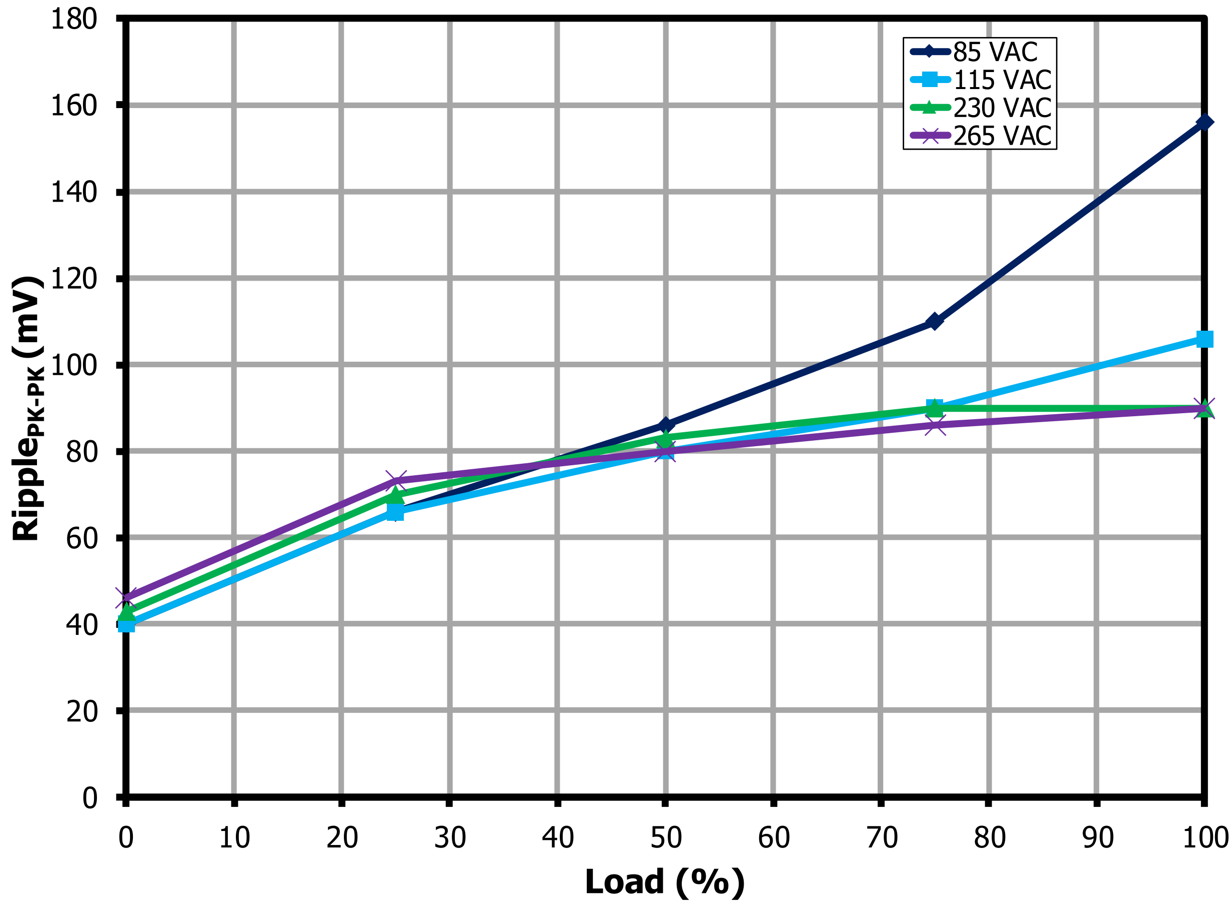

Figure 98 – Output Voltage Ripple Plots for 9 V.

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12.3.1.7 Output Voltage Ripple Plots for 3 V (End of Type-C Cable)

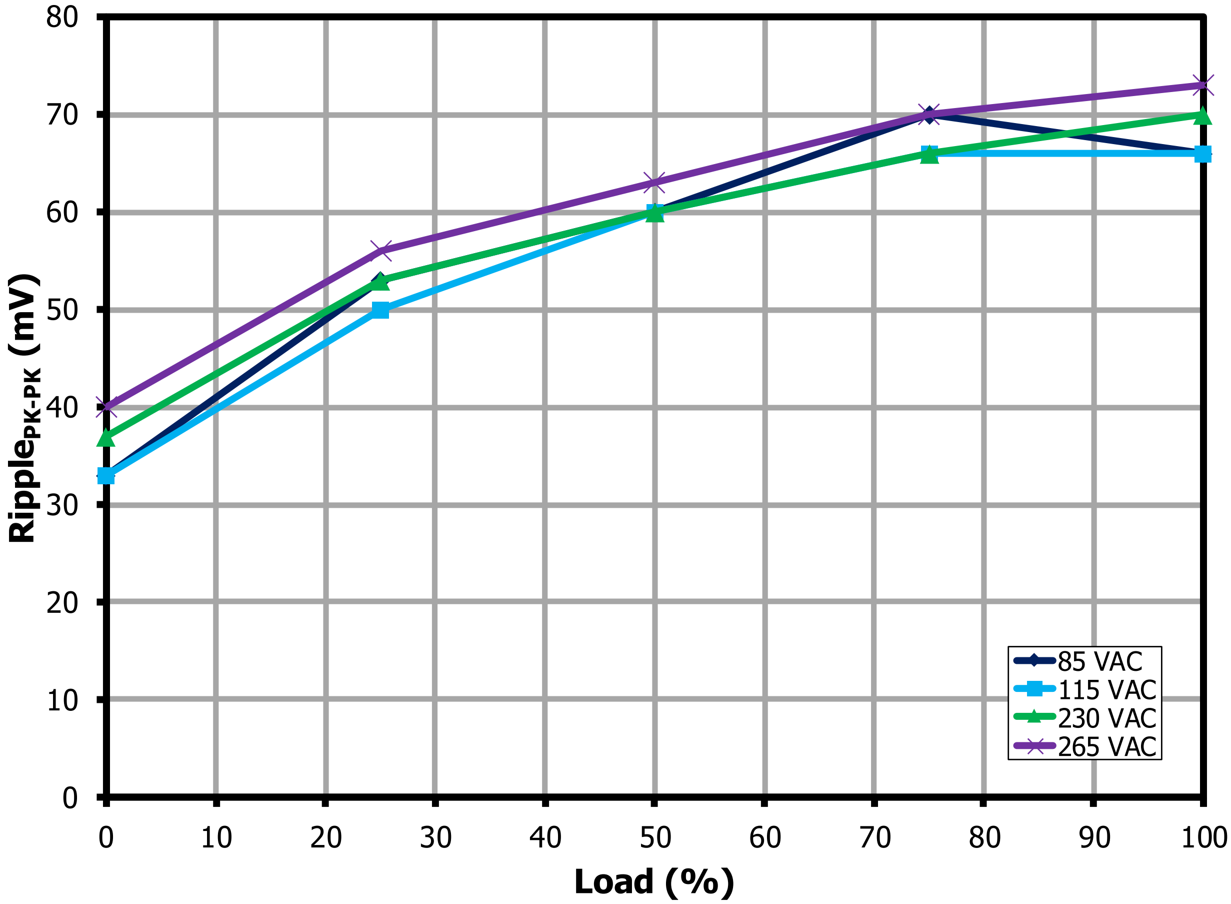

Figure 99 – Output Voltage Ripple Plots for 3 V.

12.3.1.8 Output Voltage Ripple Plots for 11 V (End of Type-C Cable)

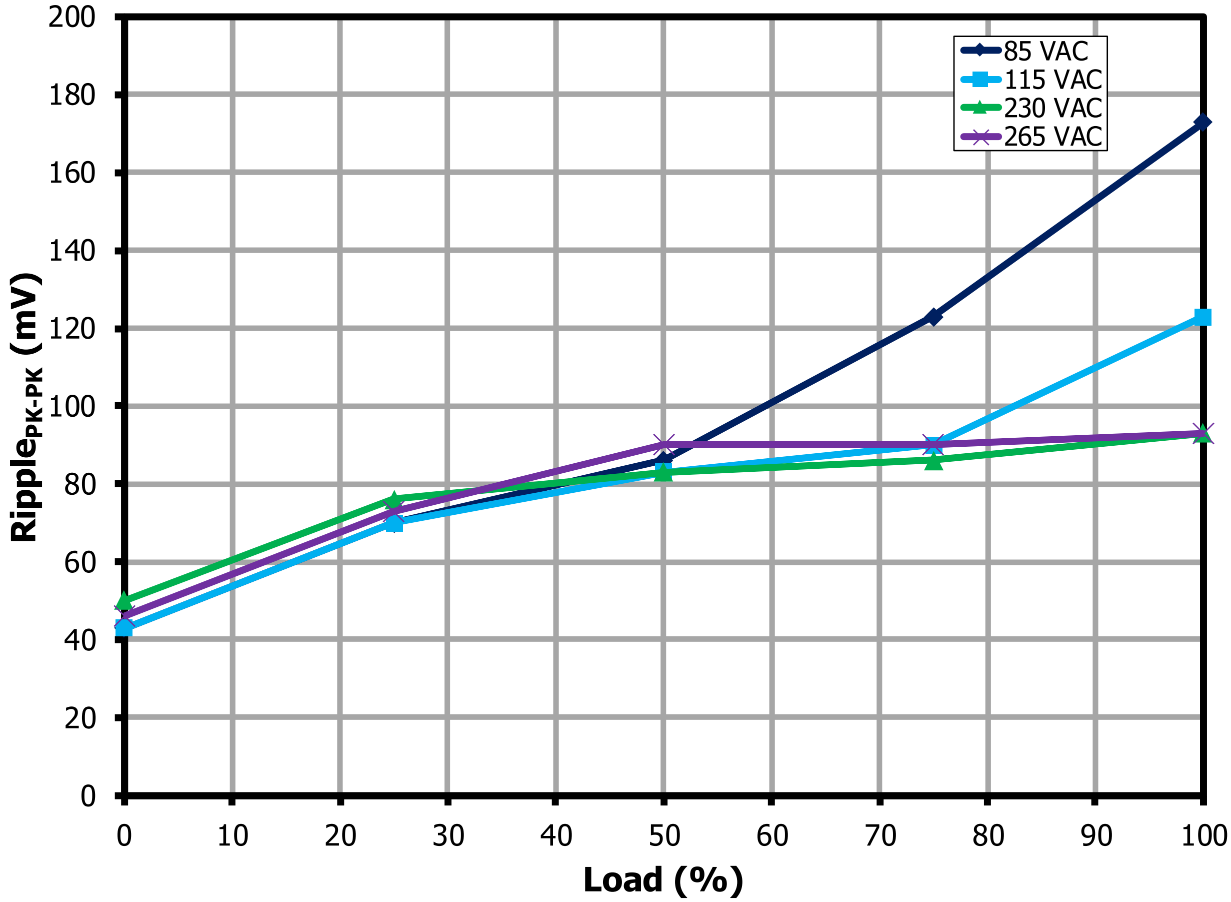

Figure 100 – Output Voltage Ripple Plots for 11 V.

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13 PPS Compliance Test

13.1 Current Limit Test

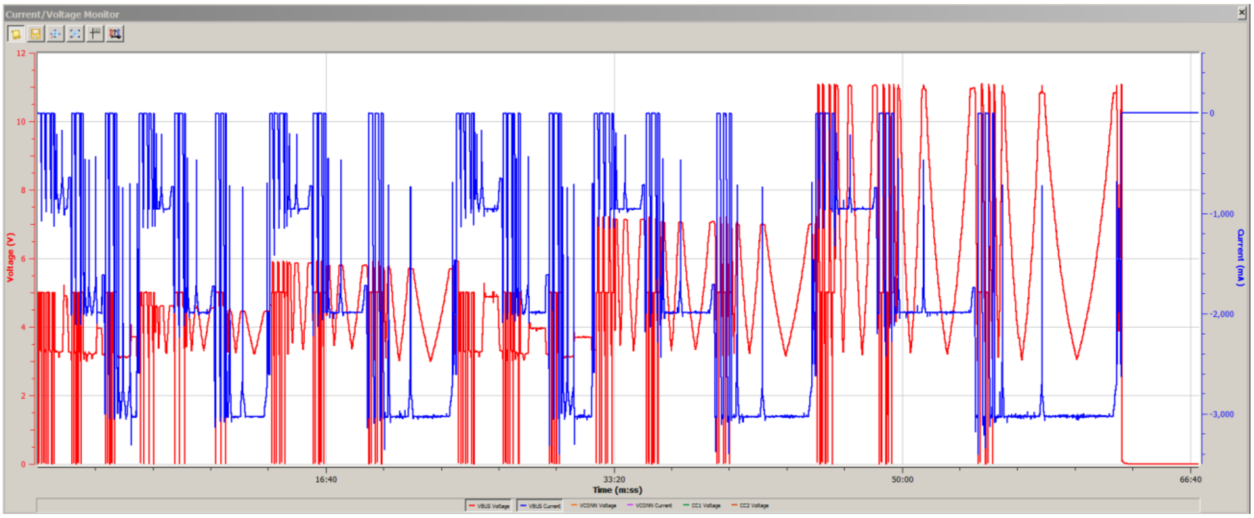

Figure 101 Total Phase Log for Quadramax Test – CLT

13.2 Voltage Step Test

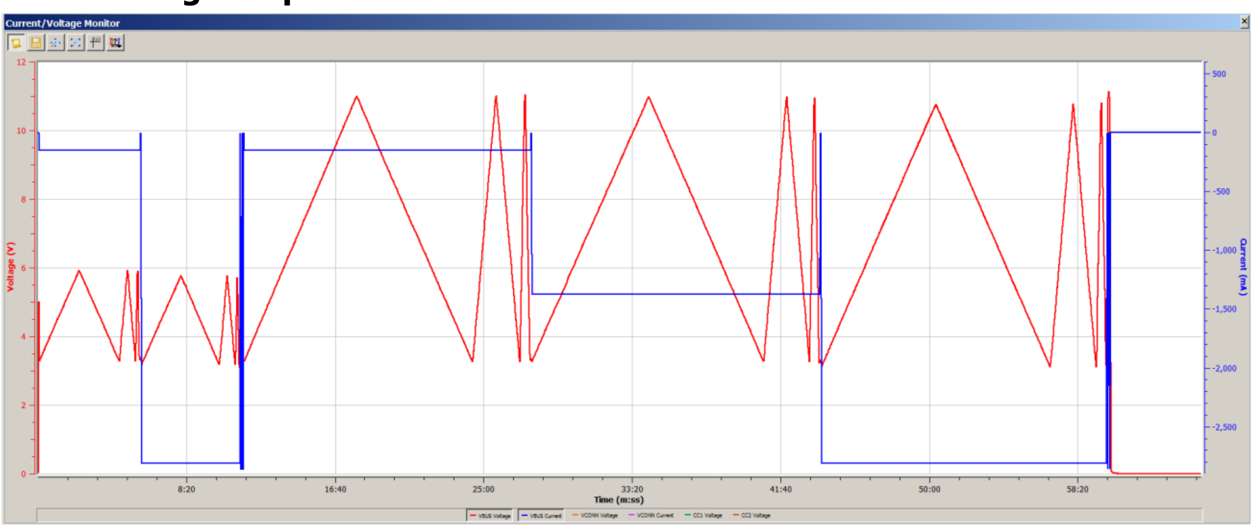

Figure 102 Total Phase log for Quadramax Test - VST

14 Thermal Performance in Open Case

14.1 85 VAC Input 5 V, 3 A

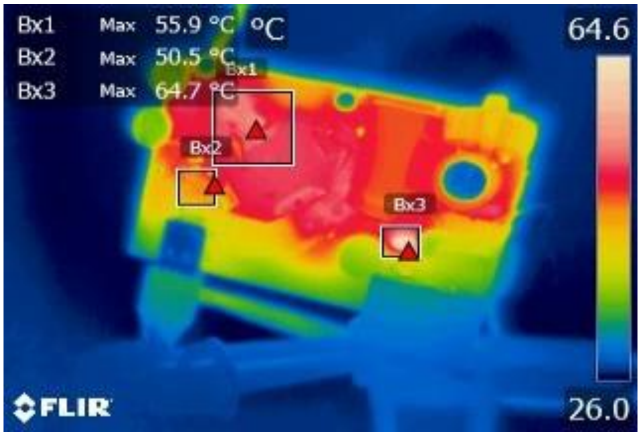

Figure 103 – Top Components, Ambient = 26 ºC.
Bx1: Transformer Secondary = 55.9 ºC.
Bx2: CCG3PA, U2 = 50.5 ºC.
Bx3: Thermistor, RT1 = 64.7 ºC.

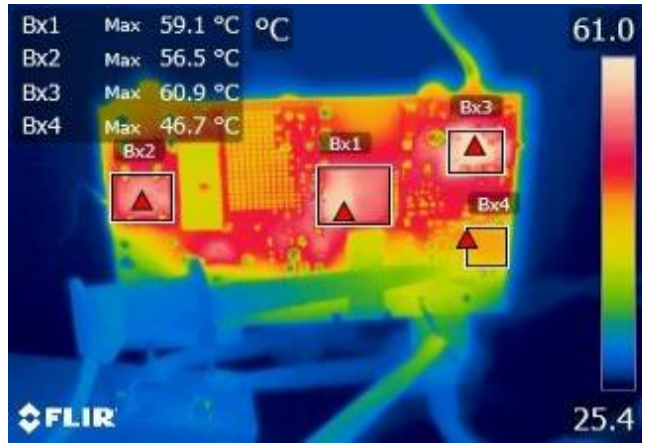

Figure 104 – Bottom Components, Ambient = 26 ºC.
Bx1: InnoSwitch3, U1 = 59.1 ºC.
Bx2: Bridge Rectifier, BR1 = 56.5 ºC.
Bx3: SR FET, Q2 = 60.9 ºC.
Bx4: Bus Switch, Q3 = 46.7 ºC.

14.2 265 VAC Input 5 V, 3 A

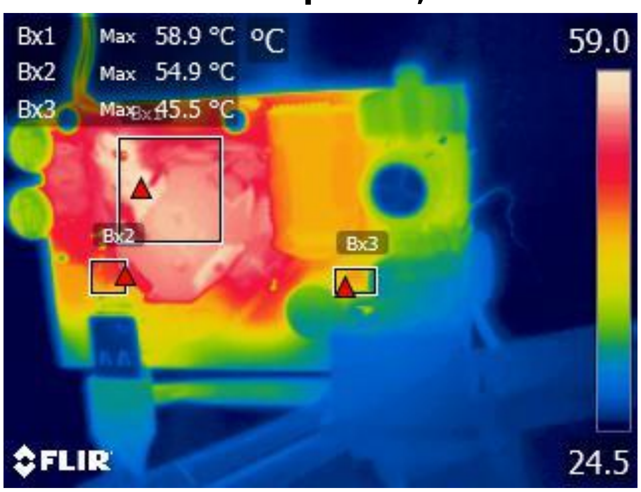

Figure 105 – Top Components, Ambient = 26 ºC.
Bx1: Transformer Secondary = 58.9 ºC.
Bx2: CCG3PA, U2 = 54.9 ºC.
Bx3: Thermistor, RT1 = 45.5 ºC.

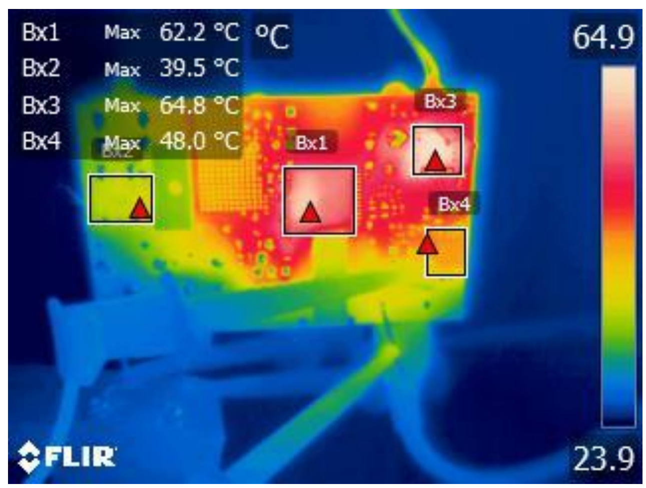

Figure 106 – Bottom Components, Ambient = 26 ºC.
Bx1: InnoSwitch3, U1 = 62.2 ºC.
Bx2: Bridge Rectifier, BR1 = 39.5 ºC.
Bx3: SR FET, Q2 = 64.8 ºC.
Bx4: Bus Switch, Q3 = 48 ºC.

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14.3 **85 VAC Input 9 V, 3 A**

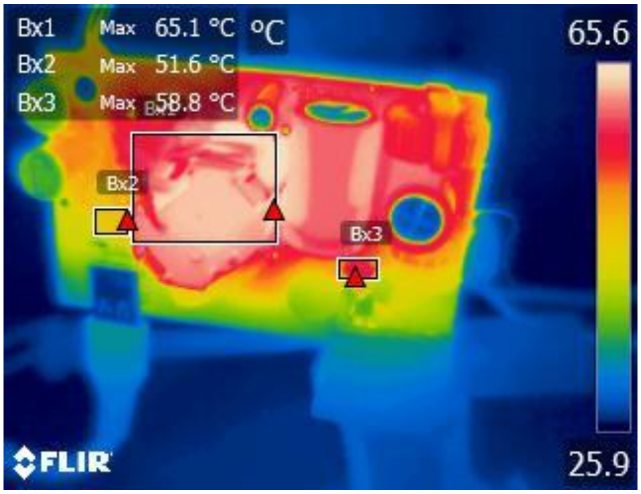

Figure 107 – Top Components, Ambient = 26.3 ºC.
Bx1: Transf. Secondary, U2 = 65.1 ºC.
Bx2: CCG3PA = 51.6 ºC.
Bx3: Thermistor, RT1 = 58.8 ºC.

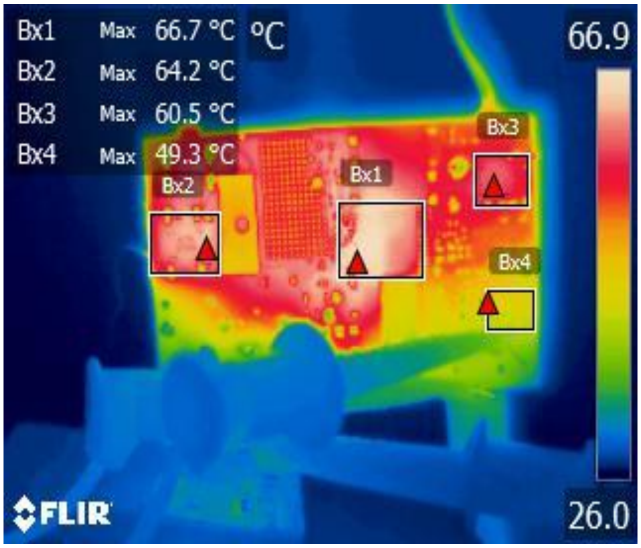

Figure 108 – Bottom Components, Ambient = 26.3 ºC.
Bx1: InnoSwitch3, U1 = 66.7 ºC.
Bx2: Bridge Rectifier, BR1 = 64.2 ºC.
Bx3: SR FET, Q2 = 60.5 ºC.
Bx4: Bus Switch, Q3 = 49.3 ºC.

14.4 **265 VAC Input 9 V, 3 A**

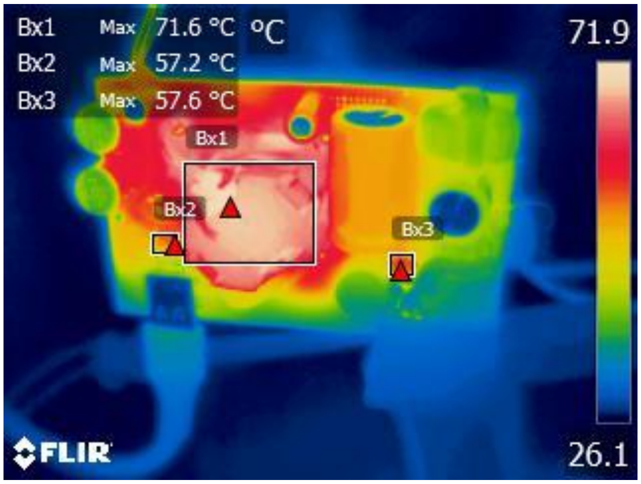

Figure 109 – Top Components, Ambient = 26.3 ºC.
Bx1: Transformer Secondary, U2 = 71.6 ºC.
Bx2: CCG3PA = 57.2ºC.
Bx3: Thermistor, RT1 = 57.6 ºC.

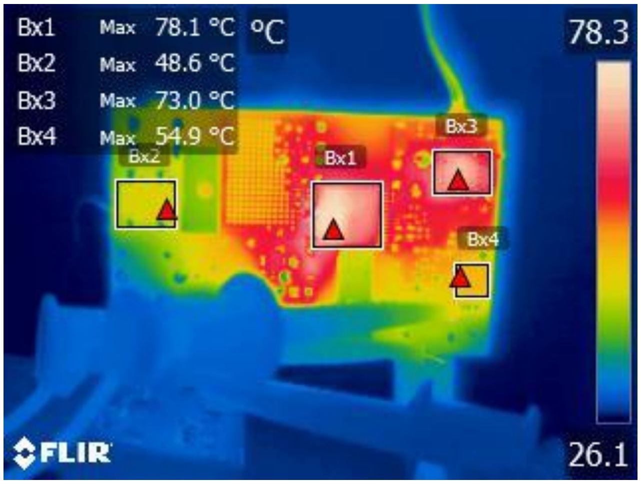

Figure 110 – Bottom Components, Ambient = 26.3 ºC.
Bx1: InnoSwitch3, U1 = 78.1 ºC.
Bx2: Bridge Rectifier, BR1 = 48.6 ºC.
Bx3: SR FET, Q2 = 73 ºC.
Bx4: Bus Switch, Q3 = 54.9 ºC.

14.5 **85 VAC Input 11 V, 2.45 A**

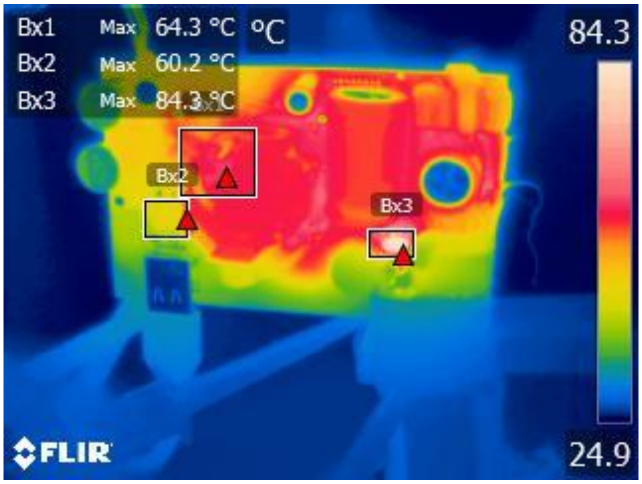

Figure 111 – Top Components, Ambient = 25.8 ºC.
Bx1: Transformer Secondary = 64.3 ºC.
Bx2: CCG3PA, U2 = 60.2 ºC.
Bx3: Thermistor, RT1 = 84.3 ºC.

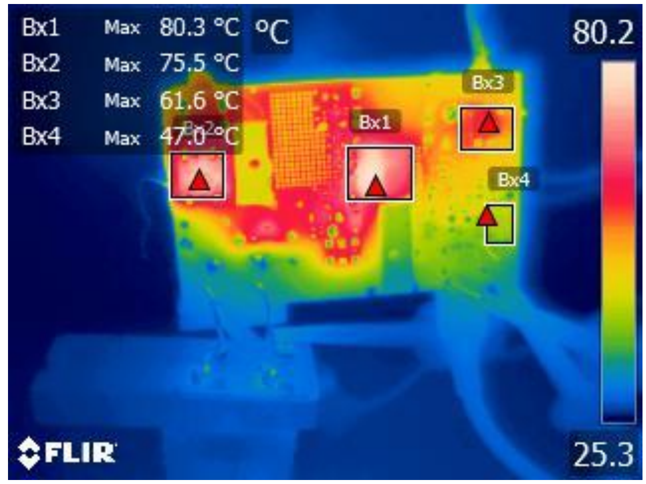

Figure 112 – Bottom Components, Ambient = 25.8 ºC.
Bx1: InnoSwitch3, U1 = 80.3 ºC.
Bx2: Bridge Rectifier, BR1 = 75.5 ºC.
Bx3: SR FET, Q2 = 61.6 ºC.
Bx4: Bus Switch, Q3 = 47 ºC.

14.6 **265 VAC Input 11 V, 2.45 A**

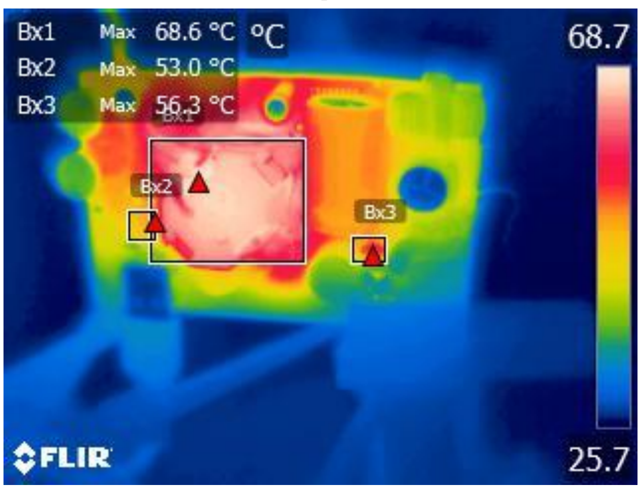

Figure 113 – Top Components, Ambient = 25.5 ºC.
Bx1: Transformer Secondary = 68.6 ºC.
Bx2: CCG3PA, U2 = 53 ºC.
Bx3: Thermistor, RT1 = 56.3 ºC.

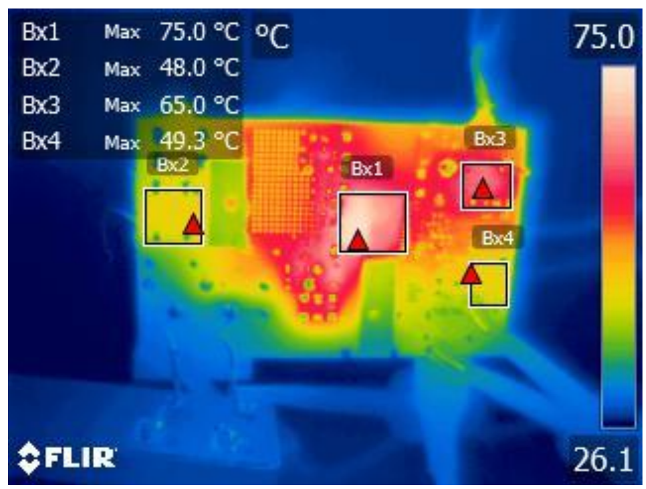

Figure 114 – Bottom Components, Ambient = 25.5 ºC.
Bx1: InnoSwitch3, U1 = 75 ºC
Bx2: Bridge Rectifier, BR1 = 48 ºC.
Bx3: SR FET, Q2 = 65 ºC.
Bx4: Bus Switch, Q3 = 49.3 ºC.

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14.7 **85 VAC Input 3 V, 3 A**

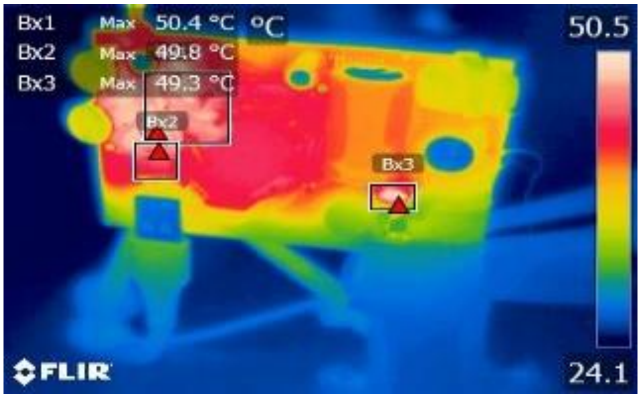


Figure 115 – Top Components, Ambient = 25.6 ºC.
Bx1: Transformer Secondary = 50.4 ºC.
Bx2: CCG3PA, U2 = 49.8 ºC.
Bx3: Thermistor, RT1 = 49.3 ºC.

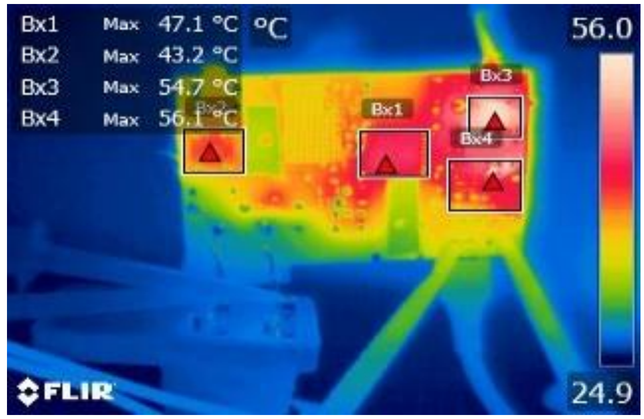


Figure 116 – Bottom Components, Amb = 25.6 ºC.
Bx1: InnoSwitch3, U1 = 47.1 ºC.
Bx2: Bridge Rectifier, BR1 = 43.2 ºC.
Bx3: SR FET, Q2 = 54.7 ºC.
Bx4: Bus Switch, Q3 = 56.1 ºC.

14.8 **265 VAC Input 3 V, 3 A**

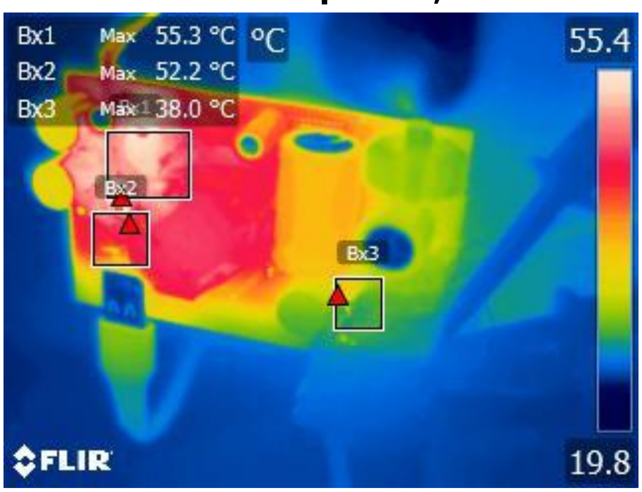


Figure 117 – Top Components, Ambient = 25.9 ºC.
Bx1: Transformer Secondary = 55.3 ºC
Bx2: CCG3PA, U2 = 52.2 ºC.
Bx3: Thermistor, RT1 = 38 ºC.

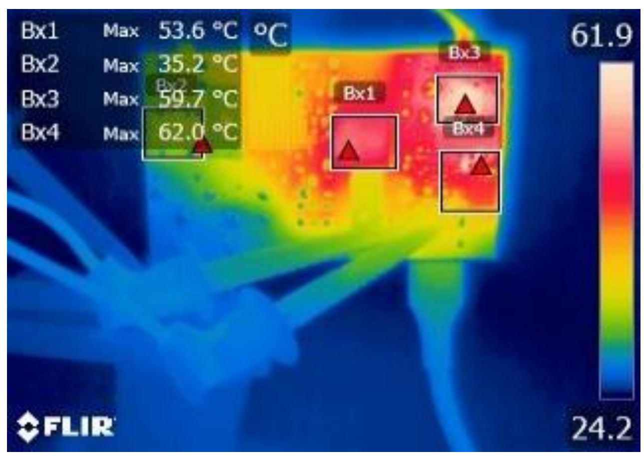
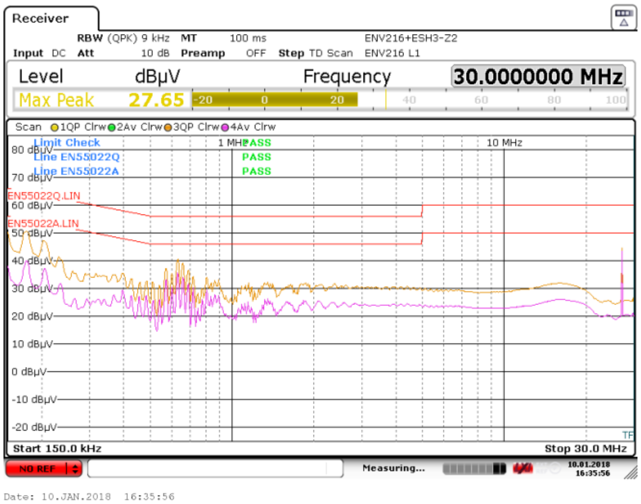


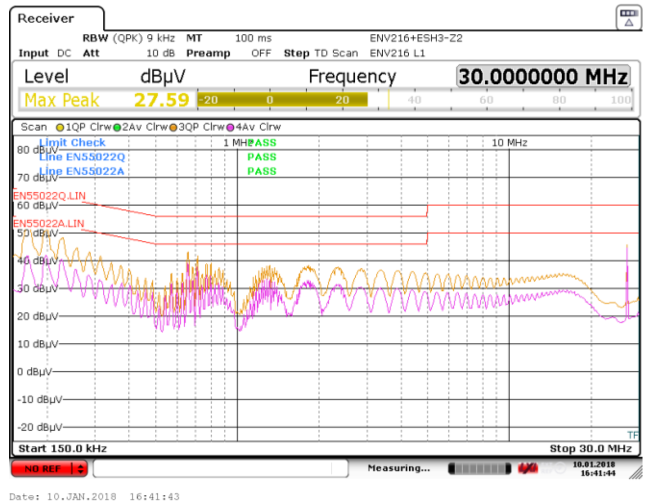
Figure 118 – Bottom Components, Ambient = 25.9 ºC.
Bx1: InnoSwitch3, U1 = 53.6 ºC.
Bx2: Bridge Rectifier, BR1 = 35.2 ºC.
Bx3: SR FET, Q2 = 59.7 ºC.
Bx4: Bus Switch, Q3 = 62 ºC.

15 Conducted EMI

15.1 Floating Output (QPK / AV)

15.1.1 *5 V, 3 A*

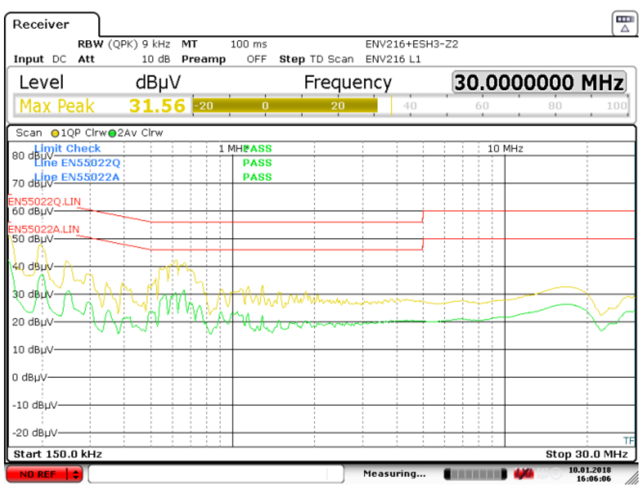




115 VAC Input 230 VAC Input

Figure 119 – Floating Ground EMI, 5 V / 3 A Load.

15.1.2 *9 V, 3 A*



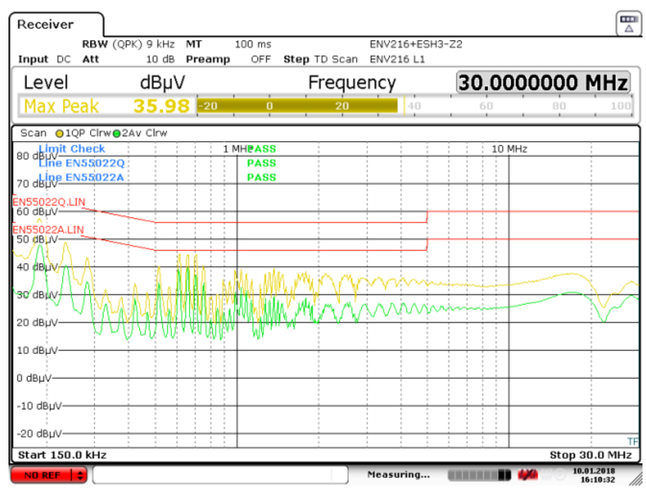


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Figure 120 – Floating Ground EMI, 9 V / 3 A Load.

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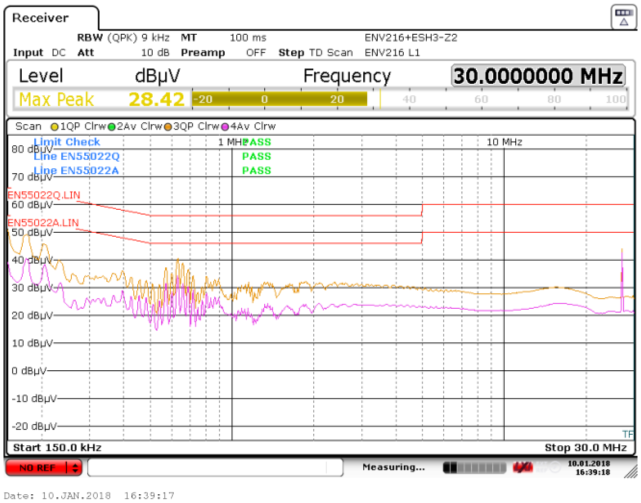
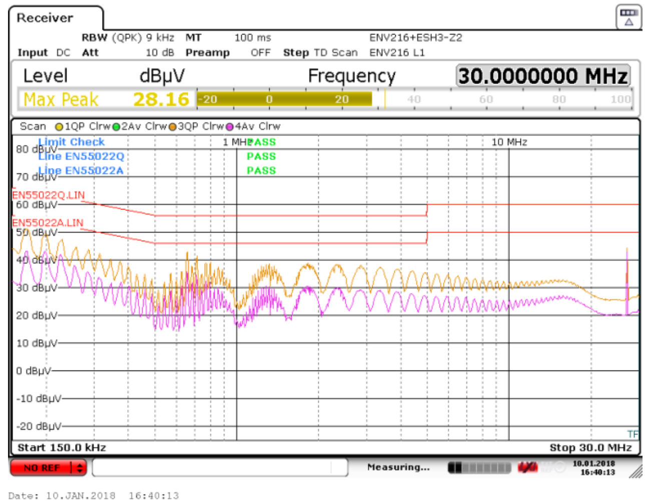
15.2 **Artificial Hand Ground (QPK / AV)**

15.2.1 *5 V, 3 A*

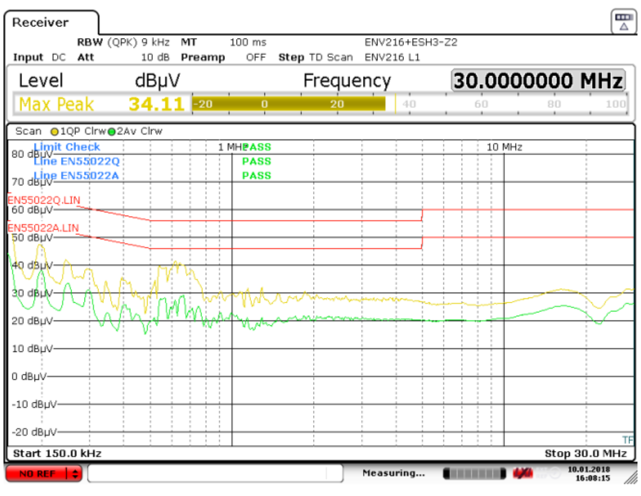


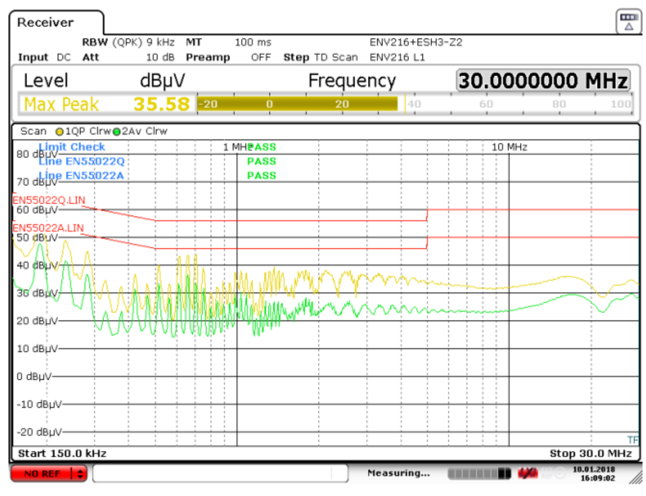


115 VAC Input 230 VAC Input

Figure 121 – Artificial Hand Ground EMI, 5 V / 3 A Load.

15.2.2 *9 V, 3 A*



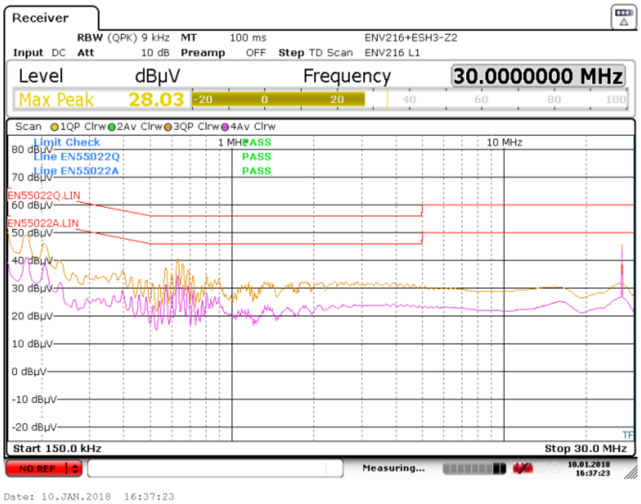


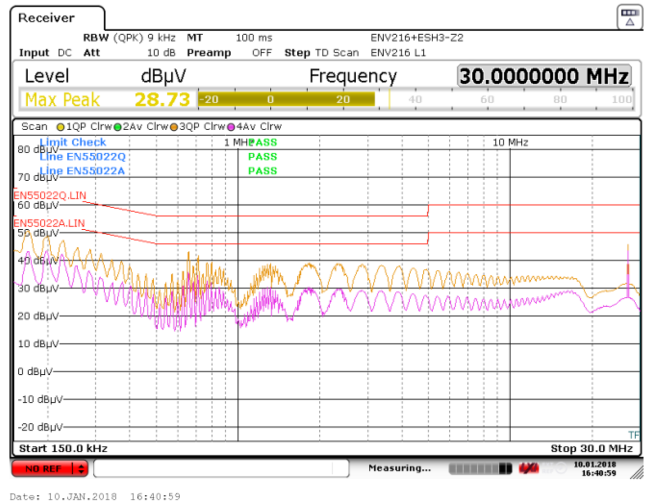
115 VAC Input 230 VAC Input

Figure 122 – Artificial Hand Ground EMI, 9 V / 3 A Load.

15.3 **Earth Ground (QPK / AV)**

15.3.1 *5 V, 3 A*

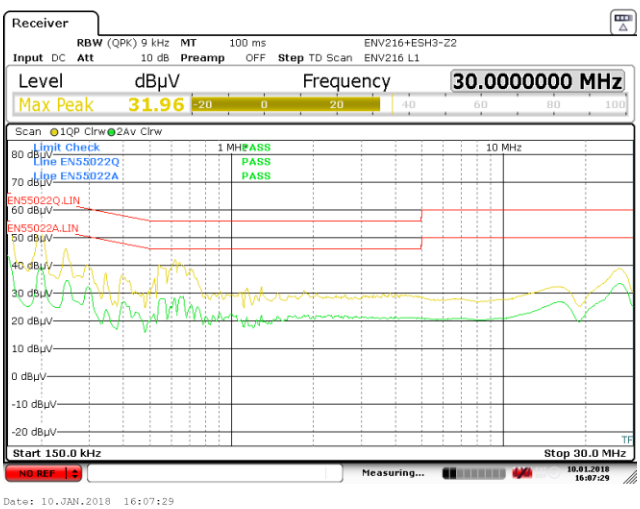


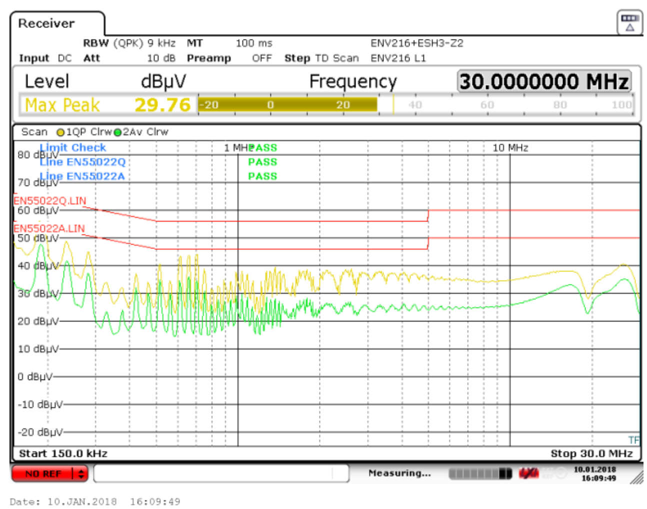


115 VAC Input 230 VAC Input

Figure 123 – Earth Ground EMI, 5 V / 3 A Load.

15.3.2 *9 V, 3 A*





115 VAC Input 230 VAC Input

Figure 124 – Earth Ground EMI, 9 V / 3 A Load.

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16 Revision History

Date	Author	Revision	Description & Changes	Reviewed
29-Dec-17	AP	1	First Draft	
30-Apr-18	RJ	1.1	Minor Updates and Review	
15-Jun-18	KM	1.2	Formatting Update	Apps & Mktg
9-Aug-18	RJ	1.3	Minor edits and added CLT,VST results	Apps & Mktg

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